# Table of Contents

## About this Manual ................................................................. 9
- Overview of Contents ......................................................... 9
- Abbreviations ........................................................................ 10
- Conventions ........................................................................... 12
- Summary of Changes ............................................................. 14

## Safety Notes ........................................................................... 15

## Sicherheitshinweise ................................................................. 19

## 1 Introduction ........................................................................ 23
- 1.1 Overview ............................................................................ 23
- 1.2 Hardware Components ...................................................... 23
- 1.3 Software Components ....................................................... 24
- 1.4 Standard Compliances ....................................................... 26
- 1.5 Ordering/Support Information ............................................ 26

## 2 Functional Description ......................................................... 29
- 2.1 Introduction ........................................................................ 29
- 2.2 Programming Model ........................................................... 29

## 3 Hardware Preparation and Installation ................................. 31
- 3.1 Overview ............................................................................ 31
- 3.2 Unpacking and Inspecting the Card ..................................... 31
- 3.3 Environmental, Thermal, and Power Requirements .......... 32
  - 3.3.1 Environmental and Thermal Requirements .................... 32
  - 3.3.2 Power Requirements .................................................... 33
- 3.4 Card Installation and Removal .......................................... 33
  - 3.4.1 Installation ............................................................... 33
  - 3.4.2 Removal ................................................................. 34

## 4 Software Installation .............................................................. 35
- 4.1 Prerequisites ....................................................................... 35
# Table of Contents

4.2 Installing Software ......................................................... 36
4.3 SharpMedia PCIE-8120 Software Package .................................. 36
  4.3.1 Library ........................................................................ 36
4.4 Configuration Overview .......................................................... 38
  4.4.1 Initialization of the Card .................................................. 38
  4.4.2 Setting up the Host ........................................................ 38
    4.4.2.1 Configuring the IP Address .......................................... 39
  4.4.3 Starting the DSPs ........................................................... 39
  4.4.4 Command Line Utility ...................................................... 40
    4.4.4.1 Octmezz Tool Usage .................................................. 40
        4.4.4.1.1 Options .......................................................... 43
        4.4.4.1.2 Examples of octmezz Tool Commands ...................... 43
    4.4.4.2 oct2200m_boot Tool Usage ........................................ 44
  4.4.5 PERL Utilities ................................................................ 46
4.5 Demo Application ............................................................... 47
  4.5.1 Executing Demo ............................................................. 47
5 Application Development .......................................................... 51
  5.1 Overview ........................................................................... 51
  5.2 Application Development Tool Kit ......................................... 51
    5.2.1 Octasic Linux Tools ...................................................... 52
  5.3 Octasic DSP Firmware Image ............................................... 52
    5.3.1 Octasic DSP Firmware image creation ............................ 53
    5.3.2 12xDSP Audio Transcode Demo .................................... 56
A PCIE-8120 External Connectors ...................................................... 57
  4.1 Overview ........................................................................... 57
  4.2 SharpMedia PCIE-8120 Card Edge Connector ......................... 58
  4.3 J1/J2 External Ethernet Connector Status LEDs (not available on -N versions) ..... 59
  4.4 P2 External ATX 6-pin Power Connector (only on -N versions) ...... 60
  4.5 Debug Connectors ............................................................. 60
  4.6 P3 Fan Unit Connector (optional component) .......................... 60
B PCIE-8120 Hardware Description ...................................................... 63
  4.1 Overview ........................................................................... 63
# Table of Contents

B.2 PCIE-8120 Card Block Diagrams ........................................... 63  
B.3 Card Reset Architecture ................................................... 66  
B.4 Power Supply Architecture ................................................. 67  
B.5 Card Clock Architecture ................................................... 68  
B.6 Ethernet NIC ................................................................. 68  
  B.6.1 NV-Memory-NIC Configuration ...................................... 69  
B.7 Ethernet Switch Unit ....................................................... 69  
  B.7.1 Main Switch Unit (MSW) - BCM5396. ............................... 69  
  B.7.2 Video Switch Unit (VSW) - BCM5396 ............................... 69  
  B.7.3 Ethernet Port Mappings ................................................ 70  
B.8 Media Flow Aggregator (MFA) Unit ....................................... 72  
B.9 Glue Logic - CPLD .......................................................... 73  
  B.9.1 Card Power Management .............................................. 73  
  B.9.2 Interfaces and Software Control .................................... 74  
    B.9.2.1 MDIO .......................................................... 74  
    B.9.2.2 Card Variant MOD_ID ......................................... 74  
    B.9.2.3 Card BASE_ID ................................................ 74  
    B.9.2.4 Opus Debug Port Multiplexer ................................. 75  
    B.9.2.5 SMBus and PVT_I2C Bus ...................................... 75  
    B.9.2.6 Debug LED .................................................... 78  
  B.9.3 CPLD Upgrade .......................................................... 79  
B.10 DSP Array ........................................................................ 80  
  B.10.1 DSP Overview ........................................................... 80  
  B.10.2 DDR3 Memory Subsystem ............................................. 81  
  B.10.3 Ethernet MAC Engines ............................................... 81  
  B.10.4 Boot Controller ......................................................... 81  
  B.10.5 DSP Configuration ...................................................... 82  
  B.10.6 DSP 25MHz Clock Synchronization ............................... 83  
  B.10.7 OPUS Debug Port ...................................................... 83  

C  Known Issues ....................................................................... 85  
  C.1 OctSetup Known Issues ..................................................... 85  
  C.2 DSP Known Issues .......................................................... 85  

D  Miscellaneous ..................................................................... 87  
  D.1 OctSetup: Internal Behavior ............................................. 87  
  D.2 Identifying Cards on the PCI-Bus ..................................... 89
# Table of Contents

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>D.3 Card Serial Number</td>
<td>90</td>
</tr>
<tr>
<td>D.4 Switches Flow Control</td>
<td>90</td>
</tr>
<tr>
<td>D.5 Verify Flow Control</td>
<td>91</td>
</tr>
<tr>
<td>D.6 Disable Flow Control</td>
<td>92</td>
</tr>
<tr>
<td>D.7 12xDSP Audio Transcode VoIP Channel Demo Application</td>
<td>92</td>
</tr>
<tr>
<td>D.7.1 Requirements</td>
<td>93</td>
</tr>
<tr>
<td>D.7.2 Running Software</td>
<td>93</td>
</tr>
<tr>
<td>D.7.2.1 New features</td>
<td>93</td>
</tr>
<tr>
<td>E Octasic Tools Package</td>
<td>97</td>
</tr>
<tr>
<td>E.1 Overview</td>
<td>97</td>
</tr>
<tr>
<td>F Install &amp; Configure PCIE-8120 in MaxCore™</td>
<td>99</td>
</tr>
<tr>
<td>F.1 Overview</td>
<td>99</td>
</tr>
<tr>
<td>F.2 Installing Software and Configuring a PCIE-8120 Card in MaxCore</td>
<td>99</td>
</tr>
<tr>
<td>G Related Documentation</td>
<td>107</td>
</tr>
<tr>
<td>G.1 SMART Embedded Computing Documentation</td>
<td>107</td>
</tr>
<tr>
<td>G.2 Related Specifications</td>
<td>107</td>
</tr>
</tbody>
</table>
## List of Figures

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-1</td>
<td>Software Diagram</td>
<td>25</td>
</tr>
<tr>
<td>1-2</td>
<td>Mechanical Layout</td>
<td>27</td>
</tr>
<tr>
<td>5-1</td>
<td>Octasic Firmware Image</td>
<td>52</td>
</tr>
<tr>
<td>5-2</td>
<td>Files in firmware build</td>
<td>54</td>
</tr>
<tr>
<td>A-1</td>
<td>PCIE-8120 Primary and Secondary Layout</td>
<td>57</td>
</tr>
<tr>
<td>B-1</td>
<td>Card Block Diagram SharpMedia PCIE-8120-A12/V12</td>
<td>63</td>
</tr>
<tr>
<td>B-2</td>
<td>Card Block Diagram SharpMedia PCIE-8120-A04</td>
<td>64</td>
</tr>
<tr>
<td>B-3</td>
<td>Card Block Diagram SharpMedia PCIE-8120-A/V12-N/-N-PP</td>
<td>65</td>
</tr>
<tr>
<td>B-4</td>
<td>Card Reset Diagram</td>
<td>66</td>
</tr>
<tr>
<td>B-5</td>
<td>Board Power Supply Architecture</td>
<td>67</td>
</tr>
<tr>
<td>B-6</td>
<td>Card Clock Scheme</td>
<td>68</td>
</tr>
<tr>
<td>B-7</td>
<td>Port Mapping PCIE-8120-A12/V12</td>
<td>70</td>
</tr>
<tr>
<td>B-8</td>
<td>Port Mapping PCIE-8120-A04</td>
<td>71</td>
</tr>
<tr>
<td>B-9</td>
<td>Port Mapping PCIE-8120-A/V12-N/-N-PP</td>
<td>72</td>
</tr>
<tr>
<td>B-10</td>
<td>SMBus and PVT_I2C bus connection diagram</td>
<td>75</td>
</tr>
<tr>
<td>B-11</td>
<td>Temperature Sensor Location</td>
<td>76</td>
</tr>
<tr>
<td>D-1</td>
<td>Host Network Setup</td>
<td>87</td>
</tr>
<tr>
<td>D-2</td>
<td>Block Diagram</td>
<td>92</td>
</tr>
</tbody>
</table>
List of Tables

Table 1-1  Standard Compliances ................................................................. 26
Table 3-1  Environmental and Thermal Requirements ........................................ 32
Table 3-2  Wattage Status ............................................................................... 33
Table 3-3  Power Requirements ...................................................................... 33
Table 4-1  Support Package RPM Files ............................................................ 36
Table 4-2  octmezz tool supported commands .................................................. 40
Table 4-3  oct2200m_boot tool supported commands ....................................... 45
Table A-1  SharpMedia PCIE-8120 Card Edge Connector Pin out ....................... 58
Table A-2  ATX PWR Pinout .......................................................................... 60
Table A-3  Optional Fan Unit Connector Pinout ................................................. 61
Table B-1  Card Variant MOD_ID .................................................................... 74
Table B-2  Sensor alert default values ............................................................... 78
Table B-3  LED Error Code (For 0, 1 and 2) ....................................................... 78
Table B-4  LED Error Code (For 3, 4, 5,6 and 7) ............................................... 79
Table B-5  Ethernet Physical Interface Mapping ............................................... 81
Table B-6  DSP Control Signals ...................................................................... 82
Table E-1  Octasic Tools Package - Directory Structure .................................. 97
Table G-1  SMART EC - Embedded Computing Publications ............................ 107
Table G-2  Related Specifications .................................................................. 107
About this Manual

Overview of Contents

This manual is divided into the following chapters and appendices.

Safety Notes on page 15 describes the safety information which has to be regarded.

Sicherheitshinweise on page 19 provides a German translation of the chapter Safety Notes.

Introduction on page 23 gives a brief overview of the product features, standard safety compliances and ordering information.

Functional Description on page 29 describes media processing functions of the component.

Hardware Preparation and Installation on page 31 includes a procedure for unpacking the product, environmental and power requirements, additional required equipment, installation, and removal instructions.

Software Installation on page 35 includes prerequisites, software packages, software installation, and demo application.

Application Development on page 51 includes application development kit, octasic Digital Signal Processor (DSP) firmware image creation, and 12xDSP audio transcode demo application.

Appendix A, PCIE-8120 External Connectors on page 57 describes the board layout, board LEDs, and connectors.

Appendix B, PCIE-8120 Hardware Description on page 63 includes block diagrams and functional description of major components.

Appendix C, Known Issues on page 85 describes known issues of octSetup and DSP connection.

Appendix D, Miscellaneous on page 87 describes octSetup, card identification on PCI-Bus, and Serial number of the card.

About this Manual

Appendix F, Install & Configure PCIE-8120 in MaxCore™ on 99 describes how to install the required SharpMedia PCIE-8120 RPMs and how to configure a PCIE-8120 card in a MaxCore system.

Appendix G, Related Documentation on 107 provides a listing of related product documentation, manufacturer’s documents and industry standard specifications.

Abbreviations

This document uses the following abbreviations:

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>API</td>
<td>Application Programmers Interface</td>
</tr>
<tr>
<td>ATX</td>
<td>Advanced Technology Extended</td>
</tr>
<tr>
<td>BGA</td>
<td>Ball Grid Array</td>
</tr>
<tr>
<td>CEM</td>
<td>Card Electro Mechanical</td>
</tr>
<tr>
<td>CISPR</td>
<td>Comité Internationale Spécial des Perturbations Radioelectrotechnique</td>
</tr>
<tr>
<td>CPLD</td>
<td>Complex Programmable Logic Device</td>
</tr>
<tr>
<td>DDR</td>
<td>Double Data Rate</td>
</tr>
<tr>
<td>DHCP</td>
<td>Dynamic Host Configuration Protocol</td>
</tr>
<tr>
<td>DRAM</td>
<td>Dynamic Random Access Memory</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processor</td>
</tr>
<tr>
<td>EMC</td>
<td>Electromagnetic Compatibility</td>
</tr>
<tr>
<td>EMV</td>
<td>Elektromagnetische Verträglichkeit</td>
</tr>
<tr>
<td>EN</td>
<td>European Norm</td>
</tr>
<tr>
<td>ETSI</td>
<td>European Telecommunications Standards Institute</td>
</tr>
<tr>
<td>FCC</td>
<td>Federal Communications Commission</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
<tr>
<td>IEC</td>
<td>International Electro technical Commission</td>
</tr>
<tr>
<td>JTAG</td>
<td>Joint Test Action Group</td>
</tr>
<tr>
<td>MAC</td>
<td>Media Access Controller</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Definition</td>
</tr>
<tr>
<td>--------------</td>
<td>------------</td>
</tr>
<tr>
<td>MDIO</td>
<td>Management Data I/O</td>
</tr>
<tr>
<td>MFA</td>
<td>Media Flow Aggregator</td>
</tr>
<tr>
<td>MGW</td>
<td>Media Gateway</td>
</tr>
<tr>
<td>NEBS</td>
<td>Network Equipment Building Standards</td>
</tr>
<tr>
<td>NIC</td>
<td>Network Interface Controller</td>
</tr>
<tr>
<td>NVRAM</td>
<td>Non-Volatile Random Access Memory</td>
</tr>
<tr>
<td>OCTVOC</td>
<td>Internal code name for Octasic DSP 1010</td>
</tr>
<tr>
<td>OCTVOC2</td>
<td>Internal code name for Octasic DSP 2224M (equipped on PCIE-8120)</td>
</tr>
<tr>
<td>OCTVOC2_EB</td>
<td>Internal code name for Octasic Evaluation Board equipped with DSP 2224M</td>
</tr>
<tr>
<td>PCI</td>
<td>Peripheral Component Interconnect</td>
</tr>
<tr>
<td>PCI-E</td>
<td>Peripheral Component Interconnect Express</td>
</tr>
<tr>
<td>PHY</td>
<td>Physical Layer Access Device</td>
</tr>
<tr>
<td>SELV</td>
<td>Safety Extra Low Voltage</td>
</tr>
<tr>
<td>SerDes</td>
<td>Serializer-Deserializer</td>
</tr>
<tr>
<td>SGMII</td>
<td>Serialized Gigabit Media Independent Interface</td>
</tr>
<tr>
<td>SMBus</td>
<td>System Management Bus</td>
</tr>
<tr>
<td>SPI</td>
<td>Serial Protocol Interface</td>
</tr>
<tr>
<td>TPE</td>
<td>Twisted-Pair Ethernet</td>
</tr>
<tr>
<td>TFTP</td>
<td>Trivial File Transfer Protocol</td>
</tr>
<tr>
<td>UL</td>
<td>Underwriters Laboratories Incorporated</td>
</tr>
<tr>
<td>VCCI</td>
<td>Voluntary Control Council for Interference</td>
</tr>
<tr>
<td>VSW</td>
<td>Video Switch</td>
</tr>
</tbody>
</table>
## About this Manual

### Conventions

The following table describes the conventions used throughout this manual.

<table>
<thead>
<tr>
<th>Notation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00000000</td>
<td>Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets</td>
</tr>
<tr>
<td>0b0000</td>
<td>Same for binary numbers (digits are 0 and 1)</td>
</tr>
<tr>
<td><strong>bold</strong></td>
<td>Used to emphasize a word</td>
</tr>
<tr>
<td>Screen</td>
<td>Used for on-screen output and code related elements or commands.</td>
</tr>
<tr>
<td><strong>Courier + Bold</strong></td>
<td>Used to characterize user input and to separate it from system output</td>
</tr>
<tr>
<td><strong>Reference</strong></td>
<td>Used for references and for table and figure descriptions</td>
</tr>
<tr>
<td>File &gt; Exit</td>
<td>Notation for selecting a submenu</td>
</tr>
<tr>
<td><code>&lt;text&gt;</code></td>
<td>Notation for variables and keys</td>
</tr>
<tr>
<td><code>[text]</code></td>
<td>Notation for software buttons to click on the screen and parameter description</td>
</tr>
<tr>
<td>...</td>
<td>Repeated item for example node 1, node 2, ..., node 12</td>
</tr>
<tr>
<td>. . .</td>
<td>Omission of information from example/command that is not necessary at the time</td>
</tr>
<tr>
<td>..</td>
<td>Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers)</td>
</tr>
<tr>
<td></td>
<td>Logical OR</td>
</tr>
<tr>
<td>![Exclamation Mark]</td>
<td>Indicates a hazardous situation which, if not avoided, could result in death or serious injury</td>
</tr>
<tr>
<td>![Exclamation Mark]</td>
<td>Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury</td>
</tr>
<tr>
<td>Notation</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>-------------</td>
</tr>
<tr>
<td>![Warning Icon]</td>
<td>Indicates a property damage message</td>
</tr>
<tr>
<td>![Caution Icon]</td>
<td>Indicates a hot surface that could result in moderate or serious injury</td>
</tr>
<tr>
<td>![Electrical Icon]</td>
<td>Indicates an electrical situation that could result in moderate injury or death</td>
</tr>
<tr>
<td>![ESD Icon]</td>
<td>Indicates that when working in an ESD environment care should be taken to use proper ESD practices</td>
</tr>
<tr>
<td>![Important Information]</td>
<td>No danger encountered, pay attention to important information</td>
</tr>
</tbody>
</table>
About this Manual

Summary of Changes

This manual has been revised and replaces all prior editions.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Publication Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6806800R89H</td>
<td>October 2019</td>
<td>Rebranded to SMART Embedded Computing</td>
</tr>
<tr>
<td>6806800R89G</td>
<td>January 2017</td>
<td>Updated Ordering/Support Information on page 18. Updated Table 3-3 on page 26. Updated Appendix A, P2 External ATX 6-Pin Power Connector (only on -N versions), on page 66. Updated Table B-1 on page 82 and Table B-2 on page 87. Added a new command under the section oct2200m_boot tool usage on page 49.</td>
</tr>
<tr>
<td>6806800R89F</td>
<td>November 2016</td>
<td>Added few commands in Table 4-1 on page 45.</td>
</tr>
<tr>
<td>6806800R89E</td>
<td>September 2016</td>
<td>Added a section Install and Configure PCIE-8120 in MaxCore on page 109. Updated the section Prerequisites on page 39.</td>
</tr>
<tr>
<td>6806800R89D</td>
<td>June 2016</td>
<td>Updated Table 3-1 on page 35. Added CentOS7.1 and RHEL 7.1 Installation and updated required package information.</td>
</tr>
<tr>
<td>6806800R89C</td>
<td>July 2014</td>
<td>Rebranded to Artesyn template.</td>
</tr>
<tr>
<td>6806800R89B</td>
<td>July 2013</td>
<td>Updated 6806800R89A.</td>
</tr>
<tr>
<td>6806800R89A</td>
<td>March 2013</td>
<td>Initial version.</td>
</tr>
</tbody>
</table>
Safety Notes

This section provides warnings that precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed during all phases of operation, service, and repair of this equipment. You should also employ all other safety precautions necessary for the operation of the equipment in your operating environment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

SMART Embedded Computing intends to provide all necessary information to install and handle the product in this manual. Because of the complexity of this product and its various uses, we do not guarantee that the given information is complete. If you need additional information, ask your SMART Embedded Computing representative.

The product has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by SMART Embedded Computing or persons qualified in electronics or electrical engineering are authorized to install, remove or maintain the product.

The information given in this manual is meant to complete the knowledge of a specialist and must not be used as replacement for qualified personnel.

Keep away from live circuits inside the equipment. Operating personnel must not remove equipment covers. Only factory authorized service personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment.

Do not install substitute parts or perform any unauthorized modification of the equipment or the warranty may be voided. Contact your local SMART Embedded Computing representative for service and repair to make sure that all safety features are maintained.

EMC

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications.

Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense. Changes or modifications not expressly approved by SMART Embedded Computing Embedded Communications Computing could void the user's authority to operate the
Safety Notes

Board products are tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a compliant system will maintain the required performance. Use only shielded cables when connecting peripherals to assure that appropriate radio frequency emissions compliance is maintained.

Operation

Product Damage - Surface of the Product

High humidity and condensation on the product surface causes short circuits.

Do not operate the product outside the specified environmental limits. Make sure the product is completely dry and there is no moisture on any surface before applying power.

Overheating and Product Damage

Operating the product without forced air cooling may lead to overheating and thus damage of the product.

When operating the product, make sure that forced air cooling is available in the enclosure.

Data Corruption

If power to the unit is removed while a firmware update is in progress to the card flash memory, the changes will not be saved, and worse, the flash memory may be corrupted. In such case the card is likely to remain in non-operable state and will require reconditioning by qualified repair services.

Installation

Damage of Circuits

Electrostatic discharge and incorrect installation and removal of the product can damage circuits or shorten their life.

Before touching the product or electronic components, make sure that your are working in an ESD-safe environment.

Product Damage

Incorrect installation of the product can cause damage of the product.

Only use appropriate tools when installing/removing the product to avoid damage/deformation to the card and/or PCB.
Cabling and Connectors

Product Damage

The RJ-45 connector(s) on the card are twisted-pair Ethernet (TPE) or interfaces. Connecting an E1/T1/J1 line to an Ethernet connector may damage the product.

Make sure that TPE connectors near your working area are clearly marked as network connectors.

Verify that the length of an electric cable connected to a TPE bushing does not exceed 100 m.

Make sure the TPE bushing of the product is connected only to safety extra low voltage circuits (SELV circuits).

If in doubt, ask your system administrator.

Environment

Always dispose equipment that is finally taken out of operation according to your country’s legislation and manufacturer’s instructions.
Sicherheitshinweise

Dieses Kapitel enthält Hinweise, die potentiell gefährlichen Prozeduren innerhalb dieses Handbuchs vorgestellt sind. Beachten Sie unbedingt in allen Phasen des Betriebs, der Wartung und der Reparatur des Systems die Anweisungen, die diesen Hinweisen enthalten sind. Sie sollten außerdem alle anderen Vorsichtsmaßnahmen treffen, die für den Betrieb des Produktes innerhalb Ihrer Betriebsumgebung notwendig sind. Wenn Sie diese Vorsichtsmaßnahmen oder Sicherheitshinweise, die an anderer Stelle diese Handbuchs enthalten sind, nicht beachten, kann das Verletzungen oder Schäden am Produkt zur Folge haben.


Das System erfüllt die für die Industrie geforderten Sicherheitsvorschriften und darf ausschließlich für Anwendungen in der Telekommunikationsindustrie und im Zusammenhang mit Industriesteuerungen verwendet werden.


Halten Sie sich von stromführenden Leitungen innerhalb des Produktes fern. Entfernen Sie auf keinen Fall Abdeckungen am Produkt. Nur werksseitig zugelassenes Wartungspersonal oder anderweitig qualifiziertes Wartungspersonal darf Abdeckungen entfernen, um Komponenten zu ersetzen oder andere Anpassungen vorzunehmen.


EMV

Sicherheitshinweise


Warnung! Dies ist eine Einrichtung der Klasse A. Diese Einrichtung kann im Wohnbereich Funkstörungen verursachen. In diesem Fall kann vom Betreiber verlangt werden, angemessene Maßnahmen durchzuführen.

Betrieb

Beschädigung des Produktes

Hohe Luftfeuchtigkeit und Kondensat auf der Oberfläche des Produktes können zu Kurzschlüssen führen.

Betreiben Sie das Produkt nur innerhalb der angegebenen Grenzwerte für die relative Luftfeuchtigkeit und Temperatur. Stellen Sie vor dem Einschalten des Stroms sicher, dass sich auf dem Produkt kein Kondensat befindet.

Überhitzung und Beschädigung des Produktes

Betreiben Sie das Produkt ohne Zwangsbelüftung, kann das Produkt überhitzt und schließlich beschädigt werden.

Bevor Sie das Produkt betreiben, müssen Sie sicher stellen, dass das Gerät über eine Zwangskühlung verfügt.

Fehlerhafter Datenbestand

Wenn sie die Spannungsversorgung des Produkts abschalten, während Programmdaten im Flashspeicher aktualisiert, werden, können diese Daten nicht korrekt gespeichert werden. In diesem Fall ist das Produkt mit hoher Wahrscheinlichkeit nicht mehr betriebsbereit und die Funktionsfähigkeit muß durch einen qualifizierten Reparaturdienst wieder hergestellt werden.
Sicherheitshinweise

Installation

Beschädigung von Schaltkreisen

Beschädigung des Produktes
Fehlerhafte Installation des Produktes kann zu einer Beschädigung des Produktes führen. Verwenden Sie geeignetes Werkzeug, um das Produkt zu installieren/deinstallieren. Auf diese Weise vermeiden Sie, dass das Card oder die Platine deformiert oder zerstört wird.

Kabel und Stecker

Beschädigung des Produktes
Bei den RJ-45 Steckern, die sich an dem Produkt befinden, handelt es sich um Twisted-Pair-Ethernet (TPE). Beachten Sie, dass ein versehentliches Anschließen einer E1/T1/J1-Leitung an einen TPE-Stecker das Produkt zerstören kann.

Kennzeichnen Sie deshalb TPE-Anschlüsse in der Nähe Ihres Arbeitsplatzes deutlich als Netzwerkanschluss.

Stellen Sie sicher, dass die Länge eines mit Ihrem Produkt verbundenen TPE-Kabels 100 m nicht überschreitet.

Das Produkt darf über die TPE-Stecker nur mit einem Sicherheits-Kleinspannungs-Stromkreis (SELV) verbunden werden.

Umweltschutz

Entsorgen Sie alte elektronische Baugruppen stets gemäß der in Ihrem Land gültigen Gesetzgebung und den Empfehlungen des Herstellers.
Chapter 1

Introduction

1.1 Overview

The SharpMedia™ PCIE-8120 is a media processing accelerator enables high density voice and video processing to be integrated into a rack mount server or other network appliances that feature standard PCI Express slots. The PCIE-8120 is an Octasic Digital Signal Processor (DSP) based PCI Express card running Vocallo MGW firmware.

The PCIE-8120 acceleration engine can take the place of additional servers when adding high density voice and video processing to an application. The PCIE-8120 card is designed for applications such as session border controllers (adding voice or video transcode), Media gateways, Media servers/media resource function, video/content optimization (transcode and transcoding), video communications servers, and interactive voice and video response systems.

The PCIE-8120 brings high density DSPs with embedded voice and video firmware from Octasic together with SMART EC’s strong embedded system and thermal design skill, resulting in an industry-leading media processing density for the next generation of voice and video processing systems.

The following are the key features of PCIE-8120.

- High performance media processing core based on power efficient DSPs
- Comprehensive voice and video processing firmware and programmers interface included
- Optional 2 x GbE ports (RJ-45) with network address translation (NAT) function for direct network attachment providing server off load
- Support for 720p and 1080p video conferencing (each DSP has 2 x 1 Gb/s data path)
- Designed for NEBS level 3 and ETSI telecom standards compliance when used in a suitable carrier grade enclosure that provides sufficient airflow
- Supports Opus (used by WebRTC) and SILK (used by Skype) audio codecs

1.2 Hardware Components

The following are the hardware components of PCIE-8120 card.

- Form factor
  - Full-height, full-length single slot PCIe add-in card with x4 PCIe interface
  - PCIe X4 Gen 2 electrical connection
- Card can operate from slot power or from an external connector for NEBS variant
Introduction

- Power envelope of 75W for > 4 DSP slot powered versions
- DSP core
  - Multicore Octasic OCT2224M DSPs running Vocallo
  - MGW firmware
  - Assembly variants with 4, 8, or 12 DSP building block
- External Ethernet port option
- Supports board control and management functions
- Internal Ethernet infrastructure capacity

1.3 Software Components

The following are the software components used to configure the PCIE-8120 card.

- Host Operating System: Red Hat Linux 6.x/CentOS 6.x/ CentOS 7.x
- PCIE-8120 card support software
- The Octasic Vocallo Media Gateway (MGW) application software
- Octasic debug tools
The following figure provides the architectural overview of the PCIE-8120 software:

**Figure 1-1  Software Diagram**

The PCIE-8120 support software configures the PCIE-8120 card, sets up the switches to which DSPs are connected and initializes the card.

The user application manages the Vocallo media processing services through a packet based Application Programmers Interface (API). The portable transport API library allows user applications to interact with the packet interface.
Introduction

1.4 **Standard Compliances**

This product is designed to meet the following standards when installed in an appropriate system environment.

<table>
<thead>
<tr>
<th>Standard</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>UL 60950-1</td>
<td>Legal safety requirements</td>
</tr>
<tr>
<td>EN 60950-1</td>
<td></td>
</tr>
<tr>
<td>IEC 60950-1</td>
<td></td>
</tr>
<tr>
<td>CAN/CSA C22.2 No 60950-1</td>
<td></td>
</tr>
<tr>
<td>CISPR 22</td>
<td></td>
</tr>
<tr>
<td>CISPR 24</td>
<td></td>
</tr>
<tr>
<td>EN 55022</td>
<td></td>
</tr>
<tr>
<td>EN 55024</td>
<td></td>
</tr>
<tr>
<td>FCC Part 15</td>
<td>EMC requirements (legal) on system level (predefined SMART Embedded Computing system)</td>
</tr>
<tr>
<td>Industry Canada ICES-003</td>
<td></td>
</tr>
<tr>
<td>VCCI Japan</td>
<td></td>
</tr>
<tr>
<td>AS/NZS CISPR 22</td>
<td></td>
</tr>
<tr>
<td>EN 300 386</td>
<td></td>
</tr>
<tr>
<td>NEBS Standard GR-1089 CORE</td>
<td></td>
</tr>
<tr>
<td>NEBS Standard GR-63-CORE</td>
<td></td>
</tr>
<tr>
<td>ETSI EN 300019 series</td>
<td>Environmental requirements</td>
</tr>
<tr>
<td>PCI-SIG CEM Rev.2.0</td>
<td>PCI Express Card Electromechanical Specification Revision2.0</td>
</tr>
</tbody>
</table>

1.5 **Ordering/Support Information**

Refer to the data sheet for the SharpMedia PCIE-8120 for a complete list of available variants and accessories. Refer to *Appendix G Related Documentation* or consult your local SMART Embedded Computing sales representative for the availability of other variants.

For technical assistance, documentation, or to report product damage or shortages, contact your local SMART EC sales representative or visit [https://www.smartembedded.com/ec/support/](https://www.smartembedded.com/ec/support/).
The outline of the SharpMedia PCIE-8120 card and its dimensions are shown in Figure 1-2. The PCB size dimensions are in accordance with the PCI-SIG CEM specifications:

- Height=101.80mm
- Length=304.50mm

Figure 1-2  Mechanical Layout
Chapter 2

Functional Description

2.1 Introduction

SharpMedia™ PCIE-8120 card is based on the Octasic OCT2224M multi-core DSP running Vocallo MGW firmware. The DSP array performs media processing acceleration for a host server, supporting both voice and video conferencing and transcode applications.

Media acceleration performance depends both on the required codecs and the number of DSPs available. A variety of board configurations allow differences in application needs and server capabilities and include a choice of 4, 8, and 12 DSPs, with maximum power consumption between 25W and 75W. An external power connector option is available only for NEBS variant.

Media streams for transcoding are typically RTP/UDP/IP streams that go to the DSP array. The functions that can be applied to each media stream are determined by the capabilities of the Vocallo MGW firmware. For more information on the media processing functions, see PCIE-8120 data sheet.

Media streams can be routed to the DSPs via the host CPU or optionally via two external Gigabit Ethernet ports provided for direct traffic termination. In this configuration, packets for transcode can bypass the host computer entirely, while a special Network Address Translation (NAT) device makes the board appear as a single IP address to external networks.

2.2 Programming Model

The internal data flows of the board are all based on Gigabit Ethernet connections with all DSPs accessible via a local Ethernet switching subsystem. Host access to all the DSPs is via a 2 x 1 Gb/s PCI Ethernet controller. The Ethernet switching subsystem also supports two 1 Gb/s links to each DSP to support special 1080p video conferencing modes. Based on the number of DSPs, this is provided by one or two on-board Ethernet switches. For more details, see the block diagrams in Appendix B, PCIE-8120 Hardware Description on page 63.

A comprehensive host-based Media Processing Application Programmers Interface is provided. This is used to configure and execute voice and video stream processing functions on the DSPs. The API commands communicate directly with the DSP array based on an endpoint and stream resource model. A nonblocking command/response protocol supports multi-channel programming efficiency.

Additional board support utilities can set the board's internal switching infrastructure into various modes, and provide diagnostic information.
Functional Description
Chapter 3

Hardware Preparation and Installation

3.1 Overview

This chapter provides information on the following topics:

- Unpacking and inspecting the card
- Environmental, thermal, and power requirements
- Card installation and removal

3.2 Unpacking and Inspecting the Card

**Electrostatic discharge and incorrect installation and removal of the card can damage circuits or shorten their life.**

**Before touching the card or electronic components, make sure that you are working in an ESD-safe environment.**

**Shipment Inspection**

To inspect the shipment, perform the following steps.

1. Verify that you have received all items of your shipment.
   - SharpMedia™ PCIE-8120 card
   - One printed copy of *Quick Start Guide*
   - One printed copy of *Safety Notes Summary*
   - Any optional items ordered

2. Remove the desiccant bag shipped with the card and dispose of it according to your country's legislation.

**The card is thoroughly inspected before shipment.**

For technical assistance or to report product damage or shortages, contact your local SMART Embedded Computing sales representative or visit [https://www.smartembedded.com/ec/support/](https://www.smartembedded.com/ec/support/).
3.3 **Environmental, Thermal, and Power Requirements**

The following environmental, thermal, and power requirements are applicable to the card.

3.3.1 **Environmental and Thermal Requirements**

You must make sure that the card, when operated in your particular system configuration, meets the environmental requirements specified below.

**NOTE:** Operating temperatures refer to the temperature of the air circulating around the card and not to the component temperature.

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Operating</th>
<th>Non-Operating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>0°C to 40°C system ambient, exceptional max. 55°C for max. 96 hours</td>
<td>-40°C to +70°C</td>
</tr>
<tr>
<td>Forced Air Flow</td>
<td>Recommended &gt;0.5 m/s</td>
<td>-</td>
</tr>
<tr>
<td>Temp. Change</td>
<td>+/-0.25°C/min</td>
<td>+/-0.25°C/min</td>
</tr>
<tr>
<td>Rel. Humidity</td>
<td>5% to 90% non-condensing</td>
<td>5% to 95% noncondensing</td>
</tr>
<tr>
<td>Vibration 5 to 200Hz</td>
<td>1g Sinusoidal</td>
<td>1g Sinusoidal</td>
</tr>
</tbody>
</table>

The PCIE-8120 temperature sensors provide alerts about absolute and delta temperature level on the card. For more information on the default values to set up sensor alarms, see Sensor Alert Default Values on page 77, and Table B-2 on page 78.
3.3.2 Power Requirements

Before installing the card, make sure that the system is capable of safely delivering the required power. Typical wattage status is given for the following operating conditions.

Table 3-2  Wattage Status

<table>
<thead>
<tr>
<th>Wattage Status</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idle</td>
<td>Card powered and is in the default reset state</td>
</tr>
<tr>
<td>Active</td>
<td>Power good status on all DSP operations</td>
</tr>
<tr>
<td>Maxload</td>
<td>Maximum load test condition (Not achieved during normal operation)</td>
</tr>
</tbody>
</table>

Table 3-3  Power Requirements

<table>
<thead>
<tr>
<th></th>
<th>PCIE-8120-A12/V12</th>
<th>PCIE-8120-A04/V04</th>
<th>PCIE-8120-A08/V08</th>
<th>PCIE-8120-A12/V12-N_PP</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V current</td>
<td>&lt;100 mA</td>
<td>&lt;100 mA</td>
<td>&lt;100 mA</td>
<td>&lt;100 mA</td>
</tr>
<tr>
<td>Typ.Wattage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Idle</td>
<td>20W</td>
<td>12W</td>
<td>12W</td>
<td>20W</td>
</tr>
<tr>
<td>Active</td>
<td>35W</td>
<td>15W</td>
<td>15W</td>
<td>33W</td>
</tr>
<tr>
<td>Maxload</td>
<td>65W</td>
<td>25W</td>
<td>39W</td>
<td>63W</td>
</tr>
<tr>
<td>12V max. current</td>
<td>5.5A</td>
<td>2.1A</td>
<td>2.1A</td>
<td>5.3A</td>
</tr>
</tbody>
</table>

3.4 Card Installation and Removal

3.4.1 Installation

Make sure that the rack mount server area can hold the full height/full length PCIE-8120 card. The rack mount server provides snap-in fixation or screw holes.

The card requires PCIE x4 connector size. It should typically be installed in a minimum x4 wide slot, x8, or x16 slot. Verify that the I/O slot can supply power via the 12V supply rail. The PCIE-8120 card can be powered-up in any slot with minimum power supply of 25W (any x4, x8, or x16 I/O slot). However, the PCIE-8120 card must be configured as a high power device to use the full 75W. For more power-up details on PCIE-8120 card, see The product data sheet for the SharpMedia™ PCIE-8120. For the PCIE-8120, a reduced number of DSP can be taken into operation if the full 75W supply is not available.
Hardware Preparation and Installation

An external ATX power connector option is available only for NEBS variant. For this you need to order a PCIE-8120 card with an external power connector. Cards with external power connectors cannot be recognized by the host without an external power connection.

Procedure - Install the PCIE-8120 in the Server

Use the following steps to install the card into the rack mount server:

1. Use anti-static pads and attach an ESD strap to your wrist. Attach the other end of the ESD strap to an electrical ground (refer to Unpacking Guidelines). The ESD strap must be secured to your wrist and to ground throughout the procedure.

2. Identify the rack mount server to be used for installation.

3. Remove any filler panel that might fill that slot.

4. Gently push the card along the guide rails till the card is fully engaged with the connector. Avoid excessive force during this operation.

5. Connect the cables appropriately.

3.4.2 Removal

The following procedure describes how to remove the PCIE-8120 card from the rack mount server.

Procedure - Remove PCIE-8120 from Server

1. Make sure you are in an ESD safe environment.

2. Remove any cable that is connected to the card.

3. Power off the system before removing the card.

4. Gently pull the card to disconnect it from the connectors. Continue to slide the card outward along the guide rails from the rack mount server.

5. Install the filler panel.
4.1 Prerequisites

Before installing the PCIE-8120 card, make sure the following software packages are installed on your host machine:

- vconfig (This package is not required for CentOS 7.x/ RHEL 7.x)
- xinetd
- net-tools
- dhcp
- tftp-server
- pciutils
- ethtool
- policycoreutils-python (needed, if SELinux is installed and enabled)
- qt (This package is required for Octasic SDK)

Download the following packages from the SWORDS portal or contact your local SMART Embedded Computing support personnel to get them installed on your host:

- PCIE-8120 support package: PCIE8120-<version>.zip
- Octasic software package: octasic-sdk-<version>.zip
- Documentation package: PCIE8120-doc-<version>.zip

**Note:** If this package is not available, contact your local SMART Embedded Computing support personnel.

Procedure - Install Software and Run Demo

Follow the steps below for software installation:

1. Mount the card in your system.
   For information on PCIE-8120 card installation, see Card Installation and Removal on page 33.

2. Install the software.
   For software installation procedure, see Installing Software on page 36.

3. Run the demo.
   **Note:** Before starting the demo, check the known issues section in OctSetup Known Issues on page 85.
4.2 Installing Software

You must be a super user to install the packages or to execute the tools from the support package.

Procedure - Install Software Packages

1. Unpack and install the following RPM files. The contents of the RPMs are installed to the /opt/bladeservices directory.

   Table 4-1 Support Package RPM Files

<table>
<thead>
<tr>
<th>Zip File</th>
<th>Contents</th>
<th>Install Command</th>
</tr>
</thead>
<tbody>
<tr>
<td>pcie8120-&lt;version&gt;.zip</td>
<td>Support package RPM</td>
<td># rpm -ihv pcie8120-&lt;version&gt;.el6.x86_64.rpm</td>
</tr>
<tr>
<td>octasic-sdk-&lt;version&gt;.zip</td>
<td>Octasic software RPM</td>
<td># rpm -ihv sofia-sip-&lt;version&gt;.el6.x86_64.rpm</td>
</tr>
<tr>
<td></td>
<td>Support library RPM</td>
<td># rpm -ihv octasic-sdk-&lt;version&gt;.el6.x86_64.rpm</td>
</tr>
</tbody>
</table>

2. Alternatively to the command rpm –ihv, you can use:

   yum localinstall ./pcie8120-1.8.1-1.el7.centos.x86_64.rpm
   yum localinstall ./sofia-sip-1.12.11-1.el7.centos.x86_64.rpm
   yum localinstall ./octasic-sdk-3.00.01-B981.el7.centos.x86_64.rpm

3. After the installation, add /opt/bladeservices/bin to the PATH variable of the user.

   export PATH = $PATH: /opt/bladeservices/bin

4.3 SharpMedia PCIE-8120 Software Package

4.3.1 Library

The library is a C-programming interface provided for software development that provides access to the resources on the card. The components that can be accessed are:

- Switches

  The DSPs (Digital Signal Processors) are connected to the ports of the switches. You can configure the switches.
Software Installation

- CPLD

The CPLD (Complex Programmable Logic Device) provides access to functions and components of the card. The CPLD controls the reset state of the DSPs and provides access to the on-board voltage and temperature sensors.

Installing the PCIE-8120 RPM creates the following folders and files in `/opt/bladeservices`.

<table>
<thead>
<tr>
<th>Folder</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>/opt/bladeservices/bin</td>
<td>Contains tools</td>
</tr>
<tr>
<td>/opt/bladeservices/share/doc/html</td>
<td>Contains documentation</td>
</tr>
<tr>
<td>/opt/bladeservices/include</td>
<td>Includes SharpMedia PCIE-8120 header files</td>
</tr>
<tr>
<td>/opt/bladeservices/lib</td>
<td>Contains SharpMedia PCIE-8120 library</td>
</tr>
<tr>
<td>/opt/bladeservices/modules</td>
<td>Contains SharpMedia PCIE-8120 kernel module</td>
</tr>
<tr>
<td>/opt/bladeservices/share/octasic</td>
<td>Contains specific configuration files to create firmware images for the DSPs</td>
</tr>
</tbody>
</table>

Installing the Octasic RPM creates the following directories in `/opt/octasic` directory:

<table>
<thead>
<tr>
<th>Folder</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>hardware</td>
<td>Contains product-specific files that are hardware dependent, such as production and update files. Use the appropriate subdirectory for your hardware platform.</td>
</tr>
<tr>
<td>software</td>
<td>Contains the Vocallo Media Gateway C header files (include subdirectory) and companion library files. Install the complete software directory in your application.</td>
</tr>
<tr>
<td>application</td>
<td>Contains various code samples and tool source code.</td>
</tr>
<tr>
<td>bin</td>
<td>Contains OS installation files and tool executable files.</td>
</tr>
<tr>
<td>doc</td>
<td>Contains documentation and release notes related to the hardware, the Vocallo Media Gateway software, and the applications provided in the package.</td>
</tr>
</tbody>
</table>
4.4 Configuration Overview

When first initialized, the board infrastructure is initialized into a default condition and the DSPs are held in reset waiting for the rest of the system to start up.

When the DSPs are taken out of reset, DSPs send out DHCP DISCOVER messages to get a firmware image. Once the DSP retrieves its networking information from the DHCP server, a firmware image is loaded to the DSP. The DSP automatically loads a firmware image via TFTP GET, in case a boot file provided in the DHCP response from the server. Otherwise, a firmware image should be uploaded using TFTP PUT to the DSP.

The standard configuration assumes that DHCP and TFTP servers are already installed and configured on the system. The octSetup tool from the support software serves for setting up a standard configuration on both DHCP and TFTP servers locally on the system.

When the DSP has loaded the right firmware image and is running, it is ready to handle media streams according to application control.

4.4.1 Initialization of the Card

Initialize the PCIE-8120 card before you start using it. Call:

```
# pcie8120-init
PCIe-8120 Initialization
fdev00.00 ... ok.
fdev00.01 ... ok.
fdev00.02 ... ok.
```

**NOTE:** To perform the initialization of all the cards installed in the system, execute the above step once after every reboot.

4.4.2 Setting up the Host

Before setting up the host assume the default IP-address of the cards and the DSPs as 192.168.100.1.

To set up the host, perform the following steps:

1. Execute the command below:

```
# octSetup
```
The following message displays when executing octSetup for the first time and can be ignored:

SELINUX: labeling directory /var/lib/tftpboot with tftpdir _rw_t ...libsemanage.dbase_1list_query: could not query record value (No such file or directory).

2. Execute this command if you want to setup a different IP address:

```
# octSetup --ipaddr=dd.dd.dd.dd
```

### 4.4.2.1 Configuring the IP Address

The default format of `<IP-address>` is `aa.bb.cc.dd`. In that `cc` denotes subnet value. Every card in the system gets its own subnet. The subnet of each card differs from the others based on their sequence of insertion.

The subnet changes based on the formula `aa.bb.[cc+Card#].dd` and Card # denotes the number of the card. By default, the first card takes the value as zero and it increments by 1 for each card. For example, assume that `192.168.100.1` is a sample IP address.

- For the first card, the IP address will be `192.168.[100+0].1` which is equal to `192.168.100.1`
- For the second card the IP address increments to `192.168.[100+1].1` which is equal to `192.168.101.1`
- Additional cards will continue to increment by 1

The following message is displayed when executing `octSetup` for the first time and can be ignored:

SELINUX: labeling directory /var/lib/tftpboot with tftpdir _rw_t ...libsemanage.dbase_1list_query: could not query record value (No such file or directory).

**NOTE:** Execute Step 1 on page 38 or Step 2 on page 39 only once. The configuration is persistent and is retained after system reboot.

### 4.4.3 Starting the DSPs

The Octasic firmware images are stored at `/var/lib/tftpboot/pcie8120` directory.

Now, the DSPs are taken out of reset. The DSP starts loading and executing the image. You can check the `tftpboot` directory given above to evaluate whether DSPs have successfully loaded its image or not. The tftp load process is successful if every DSP has stored its MAC address-specific boot status file in `tftpboot` directory.
Software Installation

Also, the boot status file’s binary content can be analyzed to check error status, version register, and progress counter. For more information, see *Boot user guide* listed in *Octasic Tools Package - Directory Structure on page 97*.

Once the DSP firmware is loaded, you can execute the demo application.

```
# octService start all
```

### 4.4.4 Command Line Utility

#### 4.4.4.1 Octmezz Tool Usage

Octmezz is the Command Line Utility provided with SharpMedia software and is used for the following operations:

- Board specific initialization
- Switch port configuration
- VLAN configuration
- DSP control operations
- Reads board information (metadata)
- Read/writes sensor devices
- Front panel Ethernet PHY configuration

**NOTE:** The *octmezz* tool version used on PCIE-8120 is *octmezz v1.7*

**Usage:**

```
octmezz --dev=<fdev> [options] <command> [parameters...]
```

The next table shows the various *octmezz* tool supported commands.

*Table 4-2  octmezz tool supported commands*

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-h</td>
<td>--help</td>
</tr>
<tr>
<td>-s</td>
<td>--status [&lt;port&gt;]</td>
</tr>
<tr>
<td>--init</td>
<td>Performs board-specific initialization</td>
</tr>
<tr>
<td>--listdev[=names]</td>
<td>Prints list of available devices</td>
</tr>
<tr>
<td>--listport [&lt;port&gt;</td>
<td>detail</td>
</tr>
<tr>
<td>--aneg &lt;port&gt; &lt;on</td>
<td>off&gt;</td>
</tr>
<tr>
<td>Command</td>
<td>Description</td>
</tr>
<tr>
<td>-----------------------</td>
<td>---------------------------</td>
</tr>
<tr>
<td>--anrestart &lt;port&gt;</td>
<td>Restarts auto-negotiation</td>
</tr>
<tr>
<td>--fwdmask &lt;port&gt; &lt;mask&gt;</td>
<td>Set forwarding mask</td>
</tr>
<tr>
<td>--dfltvid &lt;port&gt; &lt;vid&gt;</td>
<td>Set default VLAN ID</td>
</tr>
<tr>
<td>--dfltprio &lt;port&gt; &lt;prio&gt;</td>
<td>Set default priority</td>
</tr>
<tr>
<td>--setvlan &lt;vid&gt; &lt;untag map&gt; &lt;fwd map&gt;</td>
<td>Set VLAN table entry</td>
</tr>
<tr>
<td>--getvlan &lt;vid&gt;</td>
<td>Get VLAN table entry</td>
</tr>
<tr>
<td>--unsetvlan &lt;vid&gt;</td>
<td>Invalidate VLAN table entry</td>
</tr>
<tr>
<td>--listvlans [all]</td>
<td>Lists VLAN table</td>
</tr>
<tr>
<td>--portvlan &lt;vid&gt; &lt;ports...&gt;</td>
<td>Defines VLAN on ports</td>
</tr>
<tr>
<td>--noportvlan &lt;ports...&gt;</td>
<td>Removes VLAN on ports</td>
</tr>
<tr>
<td>--vlanctrl=&lt;cmd&gt;</td>
<td>Controls 802.1Q function</td>
</tr>
<tr>
<td>cmd:</td>
<td></td>
</tr>
<tr>
<td>enable</td>
<td>Enables 802.1Q VLAN function</td>
</tr>
<tr>
<td>disable</td>
<td>Disables 802.1Q VLAN function</td>
</tr>
<tr>
<td>status</td>
<td>Displays status of 802.1Q VLAN function</td>
</tr>
<tr>
<td>--arlsearch</td>
<td>Searches ARL table</td>
</tr>
<tr>
<td>--arlwrite &lt;mac&gt;[-] &lt;vid&gt; &lt;port&gt; [&lt;mac&gt;[-] &lt;vid&gt; &lt;port&gt;]</td>
<td>Writes to ARL table</td>
</tr>
<tr>
<td>--setjmbmsk &lt;clear</td>
<td>&lt;ports...&gt;&gt;</td>
</tr>
<tr>
<td>--getjmbmsk</td>
<td>Get ports with jumbo frames enabled</td>
</tr>
</tbody>
</table>
### Software Installation

#### Table 4-2  octmezz tool supported commands (continued)

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>`--dspctrl=&lt;cmd&gt; &lt;all</td>
<td>&lt;dsps...&gt;&gt; [&lt;key&gt;]`</td>
</tr>
<tr>
<td><strong>cmd:</strong></td>
<td></td>
</tr>
<tr>
<td><code>up</code></td>
<td>Take DSPs out of reset</td>
</tr>
<tr>
<td><code>down</code></td>
<td>Put DSPs into reset</td>
</tr>
<tr>
<td><code>mac</code></td>
<td>Retrieves MAC-addresses of the DSPs</td>
</tr>
<tr>
<td><code>status</code></td>
<td>Shows whether the DSPs are in reset</td>
</tr>
<tr>
<td><code>addboot</code></td>
<td>Adds DSPs to boot VLAN</td>
</tr>
<tr>
<td><code>rmboot</code></td>
<td>Removes DSPs from boot VLAN</td>
</tr>
<tr>
<td><code>arl</code></td>
<td>Writes MAC-addresses into ARL-tables</td>
</tr>
<tr>
<td><code>param: &lt;key&gt;</code></td>
<td>Parameter key</td>
</tr>
<tr>
<td><code>vlan=&lt;vid&gt;</code></td>
<td>Defines VLAN parameter</td>
</tr>
<tr>
<td><code>--i2cctrl=&lt;cmd&gt; [&lt;dev&gt;] [&lt;args..&gt;]</code></td>
<td>I2C-bus operation</td>
</tr>
<tr>
<td><strong>cmd:</strong></td>
<td></td>
</tr>
<tr>
<td><code>read</code></td>
<td>Reads from device</td>
</tr>
<tr>
<td><code>write</code></td>
<td>Writes to device</td>
</tr>
<tr>
<td><code>list</code></td>
<td>Lists known devices</td>
</tr>
<tr>
<td><code>--mfactrl=&lt;cmd&gt;</code></td>
<td>Controls the MFA-FPGA</td>
</tr>
<tr>
<td><strong>cmd:</strong></td>
<td></td>
</tr>
<tr>
<td><code>up</code></td>
<td>Take MFA out of reset</td>
</tr>
<tr>
<td><code>down</code></td>
<td>Put MFA into reset</td>
</tr>
<tr>
<td><code>status</code></td>
<td>Shows status of MFA</td>
</tr>
<tr>
<td><code>--bdinfo</code></td>
<td>print board information</td>
</tr>
<tr>
<td><code>--extphyop=&lt;cmd&gt; &lt;FP_ETH1/FP_ETH2&gt;</code></td>
<td>Controls external PHY operation</td>
</tr>
<tr>
<td><strong>cmd:</strong></td>
<td></td>
</tr>
<tr>
<td><code>up</code></td>
<td>Enables external PHY</td>
</tr>
<tr>
<td><code>down</code></td>
<td>Disables external PHY</td>
</tr>
<tr>
<td><code>status</code></td>
<td>Shows status of ext PHY</td>
</tr>
<tr>
<td><code>--cpld_version</code></td>
<td>Shows the CPLD version</td>
</tr>
</tbody>
</table>
### 4.4.4.1.1 Options

- `--bcmreset=<cmd>`  
  - `cmd`: controls the reset functionality of switch  
  - `set`: resets the switch  
  - `clr`: brings the switch out of reset

- `--arltblclr <vid>`  
  - Clears arl table entries for specified vid

- `--flowctrl=<cmd> <port>`  
  - `cmd`: controls flow-control for the specified port  
  - `on`: enables flow-control  
  - `off`: disables flow-control

### 4.4.4.1.2 Examples of octmezz Tool Commands

- **help**  
  - Displays octmezz help message.

  ```bash
  octmezz --help
  ```

- **Devicenames**  
  - Displays list of PCIE-8120 devices available in the host system.

  ```bash
  octmezz -listdev=names
  ```

- **Port Status**  
  - Lists the status of all ports of MSW0(Main switch of PCIE-8120) device.

  ```bash
  octmezz --dev=MSW0 -s
  ```

---

**Table 4-2 octmezz tool supported commands (continued)**

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>--bcmreset=&lt;cmd&gt;</code></td>
<td>Controls the reset functionality of switch</td>
</tr>
<tr>
<td><code>cmd:</code></td>
<td></td>
</tr>
<tr>
<td><code>set</code></td>
<td>Resets the switch</td>
</tr>
<tr>
<td><code>clr</code></td>
<td>Brings the switch out of reset</td>
</tr>
<tr>
<td><code>--arltblclr &lt;vid&gt;</code></td>
<td>Clears arl table entries for specified vid</td>
</tr>
<tr>
<td><code>--flowctrl=&lt;cmd&gt; &lt;port&gt;</code></td>
<td>Controls flow-control for the specified port</td>
</tr>
<tr>
<td><code>cmd:</code></td>
<td></td>
</tr>
<tr>
<td><code>on</code></td>
<td>Enables flow-control</td>
</tr>
<tr>
<td><code>off</code></td>
<td>Disables flow-control</td>
</tr>
<tr>
<td><code>--noinit</code></td>
<td>skips board-specific initialization, this is the default command option</td>
</tr>
<tr>
<td><code>--addr=&lt;phy&gt;</code></td>
<td>use &lt;phy&gt; as address, if this command is omitted card will accept default address</td>
</tr>
<tr>
<td><code>--dev=&lt;fdev&gt;</code></td>
<td>use fdevxx.f as device string, for example, fdev00.0 is card #0 function #0 (alternatively msw0 will work)</td>
</tr>
</tbody>
</table>
Software Installation

Port Details

Lists the port details of MSW0 device.

```
octmezz --dev=MSW0 --listport detail
```

vlans

Lists the vlans of MSW0 device

```
octmezz --dev=msw0 --listvlans
```

DSP Status

Displays the status of DSPs present on the PCIE-8120 board.

```
octmezz --dev=msw0 --dspctrl=status all
```

Sensor Devices

Lists the sensor devices present on the PCIE-8120 board hosting cpld0 device.

```
octmezz --dev=cpld0 --i2cctrl=list
```

Temperature Sensors

Reads inlet temperature sensor of the PCIE-8120 board hosting cpld0 device.

```
octmezz --dev=cpld0 --i2cctrl=read t_inlet
```

Board information

Retrieves the board specific information of the given PCIE-8120 board. It fetches the information like Board serial number, Marketing number, and Assembly part number.

```
octmezz --dev=cpld0 --bdinfo
```

Front panel Ethernet Port Status

Displays the status of front panel Ethernet port connected to MSW0 device of PCIE-8120 board.

```
octmezz --dev=msw0 --extphyop=status FP_ETH1
```

4.4.4.2 oct2200m_boot Tool Usage

The `oct2200m_boot` tool can be used as an alternate method for booting the DSPs. The description about the tool is mentioned in the `oct2200m_boot.txt` file and also provided in the usage when calling the tool without any arguments.
The dhcpd and tftp.socket services need to be disabled because the tool uses its own respective functions.

    systemctl stop tftp.socket
    systemctl stop dhcpd

*oct2200m_boot tool supported commands on page 45* shows a list of various *oct2200m_boot tool supported commands*.

**Usage:** ./oct2200m_boot [option] <command> [<parameter>...]

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>reset</td>
<td>Displays octmezz tool help</td>
</tr>
<tr>
<td>boot</td>
<td>Displays status of ports</td>
</tr>
<tr>
<td>mac</td>
<td>Find MAC address of DSP(s)</td>
</tr>
<tr>
<td>info</td>
<td>Provides tool internal information for DSP(s)</td>
</tr>
</tbody>
</table>

**Options:**

- `--interface <if name>` Interface for communication with DSPs. The default value is board specific.
- `--config <file name>` Configuration file with DSP IP addresses. The default value is automatic assignment of IP addresses.
- `--timeout <value>` DSP boot timeout in ms. The default value is 1500.
- `--boot-delay <value>` Boot sequence delay in ms. The default value is 10.
- `--boot-retries <value>` Number of boot retries. The default value is 2.
- `--no-reset-after-fail` Do not put a DSP in reset if it fails to boot.
- `--verbose` Generate verbose output.
- `--timestamp` Add timestamps to verbose output.
- `--trace {dhcp|tftp} {packet|error}` Trace DHCP/TFTP packets/errors.
- `--trace bdi data` Trace BDI data exchange.

**Example Commands**

The following are the sample commands for the two interfaces *enp1s0f0* and *enp1s0f2* of card 0.

- Get information about DSPs
Software Installation

```
oct2200m_boot 0 info all

Boot all 12 DSPs of card 0 on interface enp1s0f0
oct2200m_boot -i enp1s0f0 boot 0 0-11 oct2200.img

Boot 6 DSPs of card 0 via NIC0, 6 DSPs via NIC2
oct2200m_boot -v -br 0 -i enp1s0f0 boot 0 0-4 /opt/octasic/hardware/octvoc2/oct2200/bootfile/oct2200cita
delle.img
oct2200m_boot -v -br 0 -i enp1s0f0 boot 0 7 /opt/octasic/hardware/octvoc2/oct2200/bootfile/oct2200cita
delle.img
oct2200m_boot -v -br 0 -i enp1s0f2 boot 0 5-6 /opt/octasic/hardware/octvoc2/oct2200/bootfile/oct2200cita
delle.img
oct2200m_boot -v -br 0 -i enp1s0f2 boot 0 8-11 /opt/octasic/hardware/octvoc2/oct2200/bootfile/oct2200cita
delle.img
```

The description about the options used in the above example is provided below.

- `-v` verbose output
- `-br 0` To repeat trial 0 times.
- `-i` The default interface is NIC0. -i NIC2 is required for the second group.

### 4.4.5 PERL Utilities

The PCIE-8120 software provides following PERL utilities:

- `pcie8120-boot-status` Provides information about the boot status of PCIE-8120 DSPs
- `pcie8120-dsp-boot-setup` Used internally by octSetup utility to configure/create the boot environment for DSPs to boot from host system
- `pcie8120-listdev` Lists all available PCIE-8120 cards on the host system along with PCIe bus details
- `pcie8120-serialno` Provides serial numbers of all available PCIE-8120 cards on the host system
- `octService` Used to start/stop the DSPs available on PCIE-8120 cards
- `pcie8120-init` Initializes/configures all available PCIE-8120 cards on host system
4.5 Demo Application

SMART Embedded Computing provides a demo application for the PCIE-8120 that sets up 400 IP-to-IP channels (800 IP end points) per DSP to transfer voice data from one DSP to another. The demo application monitors all DSPs (one after the other) and evaluates its status by providing statistical data.

For more information with basic examples on configuring the DSPs with various codecs, refer to Octasic SDK folder /opt/octasic/application/sample/octvoc.

NOTE: The demo is used to configure 12 DSPs.

4.5.1 Executing Demo

The demo is used to configure the maximum number of VoIP connections on the PCIE-8120.

For more information, see 12dsp_audio_transcode_net_api.c file at /opt/octasic/application/sample/octvoc/12dsp_audio_transcode_net_api/source location.

To start the demo, execute the following:

```
# cd /opt/octasic/application/sample/octvoc/12dsp_audio_transcode_net_api.
```

To execute the demo, find the MAC address of your local interface to the card. Determine the network interface with the tool pcie8120-listdev. Associate the interface with device function MSW (example output):

```
# pcie8120-listdev
PCIE-8120-A12/V12#0
   MSW0: 05:00.0 eth6
   CPLD0: 05:00.1 eth7
   VSW0: 05:00.2 eth5
```

Retrieve the MAC address of this network interface (here eth6) by executing the command ifconfig:

```
# ifconfig eth6
```
Software Installation

```
eth6  Link encap:Ethernet  HWaddr 00:80:42:2C:7B:D8
Mask:255.255.255.0
    inet6 addr: fe80::280:42ff:fe2c:7bd8/64 Scope:Link
    UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
    RX packets:2401552 errors:0 dropped:0 overruns:0 frame:0
    TX packets:36880 errors:0 dropped:0 overruns:0 carrier:0
    collisions:0 txqueuelen:0
    RX bytes:725995492 (692.3 MiB)  TX bytes:54316690 (51.8 MiB)
```

Start the demo with the MAC address retrieved above:

```
# ./12_dsp_audio_transcode_net_api 00:80:42:2C:7B:D8 1
```

The first argument defines the MAC of the MSW network interface. The second argument defines the number of iterations. In the example above, just one loop is executed. To run continuously use `-1` for the number of iterations:

```
# ./12_dsp_audio_transcode_net_api 00:80:42:2C:7B:D8 -1
```

The test passes, if all of the `Err, Drop, Slip` counters are zero. In this case the following output is provided:

```
*** Loop: 0 ***
--- VOC TERM MC STATISTICS (DSP 00) ------------------------------
| RxOutPktCnt : 2457645 |
| RxInSidPktCnt : 0 |
| RxNoPktCnt : 2448744 |
| RxBadPktTypeCnt : 0 |
| RxBadRtpPayloadTypeCnt : 0 |
| RxBadPktHdrFormatCnt : 0 |
| RxBadPktLengthCnt : 0 |
| RxMisorderedPktCnt : 0 |
| RxLostPktCnt : 0 |
| RxBadPktChecksumCnt : 0 |
| RxUnderrunSlipCnt : 0 |
| RxOverrunSlipCnt : 0 |
| RxLastVocoderType : 0 |
| RxVocoderChangeCnt : 0 |
| RxMaxDetectedPdv : 173 (in 125 us) |
| RxDecdrRate : 0 |
| RxMaxJitterCurrentDelay : 165 (in 125 us) |
| RxJitterEstimatedDelay : 0 (in 125 us) |
| RxJitterEstimatedDelay : 0 (in 125 us) |
| RxJitterClkDriftingCorrectionCnt : 0 |
```
| RxMaxJitterInitializationCnt     : 1 |
| RxCircularBufferWriteErrCnt     : 0 |
| RxApiEventCnt                   : 0 |
| TxCurrentVocoderType            : 0 |
| TxInPktCnt                      : 2456643 |
| TxInBadPktPayloadCnt            : 0 |
| TxTimestampGapCnt               : 0 |
| TdTdmWriteErrCnt                : 0 |
| RxToneDetectedCnt               : 0 |
| RxToneRelayEventPktCnt          : 0 |
| RxToneRelayUnsupportedCnt       : 0 |
| TxToneRelayEventPktCnt          : 0 |
| TxApiEventCnt                   : 0 |
| TxNoRtpEntryPktDropCnt          : 0 |
| ConnectionWaitAckFlag           : 0 |
| RxMipsProtectionDropCnt         : 0 |
| TxMipsProtectionDropCnt         : 0 |
| CallTimerMsec                   : 61665 |

**Note:** The loop counter increments, each time the DSP 00 displayed.

If any of the **Err**, **Drop**, **Slip** counters are non-zero, a warning is displayed at the end of each DSP’s statistics list.
Chapter 5

Application Development

5.1 Overview

Applications make use of both the board services tools and the media processing APIs. The board support tools are required to manage the setup and operation of the board, including bringing DSPs out of reset. The media processing application development software environment is provided by the Octasic Vocallo MGW SDK package.

During normal operation, it is also important to monitor the board temperature sensors using the board support tools in case of problems with the airflow.

5.2 Application Development Tool Kit

SMART Embedded Computing provides all the Octasic information to enable you to start application development. The following information is included in the application development tool kit:

- Octasic documentation
- Octasic VOCALLO API source files
- Octasic basic examples
- Precompiled DSP firmware image file
- Vocallo MGW SDK to match firmware image
- SMART Embedded Computing Demo application configuring all 12 DSPs on the PCIE-8120
- SharpMedia™ PCIE-8120 configuration files (csv and octvocfs.tar)
- DSP firmware creation tool executable
- Audio license file
- Debug tools

**NOTICE**

OCTVOC2 is the internal name for OCT2224M DSP devices that are used on the SharpMedia PCIE-8120 card.

Be aware that other software packages (OCTVOC=OCT3 1010 DSP, OCTVOC2_EB=OCT2224M evaluation board) should not be used with SharpMedia PCIE-8120.

For detailed documentation about the Octasic VOCALLO software, see readme.html file at the /opt/octasic/doc location.
5.2.1 Octasic Linux Tools

Octasic provides tools for development and debugging. This tool package is provided for Linux:

- **File name**: octconsole, ethloopback_test, octlifeview, wireshark plugins
- **File location**: /opt/octasic

Documentation from Octasic is provided inside the tool folders.

5.3 Octasic DSP Firmware Image

Every Octasic DSP on the S PCIE-8120 card loads the firmware code and it executes directly from external DRAM. The firmware image is loaded in the following way:

*Figure 5-1 Octasic Firmware Image*

A sample DSP firmware image is provided for quick-start only. It has been built from the Octasic source code delivered with the package `octasic-sdk`.

To get the latest version of the source code, code fixes, new codecs and appropriate license files, contact SMART EC.

Boot status can be read by evaluating the stage1- and stage2-specific boot process progress counter, version register, error status, and info field. DSP writes its boot status into `boot_status.<MAC-address>` file located in the TFTP root directory, defaults are `/var/lib/tftpcBoot` or `/tftproot`.

The write operation occurs when either the Stage2 process completes successfully just prior to entering the application, or when an error is encountered just before the Stage 2 process halts. These registers are valid only during the boot process.
5.3.1 **Octasic DSP Firmware image creation**

Octasic provides an image creation tool, that allows the user to specify configuration options and the application object file to be included when creating the bootfile. The DSP firmware image creation application is provided with the package:

**File Name:** oct2200_boot_img_gen  
**File Location:** /opt/octasic/bin  
**Syntax:** oct2200_boot_img_gen  <input file> <output file>  
**Input file:** simplified CSV description file created for PCIE-8120.  
**Output file:** firmware image file created  
**Example:**

```
# cd /opt/octasic/hardware/octvoc2/oct2200/bootfile
#/opt/octasic/bin/oct2200_boot_img_gen
  octvocmgw.citadelle.csv oct2200citadelle.img
```

---

**NOTICE**

The firmware image provided cannot be used with other revisions of Octasic VOCALLO APIs. It includes an audio license only. You need to create new firmware images with every new release or when changing precompiled options.

---

**NOTICE**

Always use the octvocmgw.citadelle.csv file provided with the RPM for creating DSP images for SharpMedia PCIE-8120. To set up the card with its board-specific hardware, octvocmgw.citadelle.csv file is required.
The following figure shows the files included in a firmware build and the files that should be configured with reference to the application:

**Figure 5-2  Files in firmware build**

- **Input file** `octvocmgw.citadelle.csv` includes a TAR file called `octvocfs.tar`. The tar file contains two files:
  - license file (audio license) `octvc1.lic.asc`
  - hardware/application configuration file `octvc1_config.arg`

The file `octvc1_config.arg`, located in folder `octvocmgw`, specifies the hardware specifics of the SharpMedia PCIE-8120.

```xml
<EthernetPort PortNum="0">
  <PortInterface Value="EMAC2"/>
</EthernetPort>
<EthernetPort PortNum="1">
  <PortInterface Value="EMAC0"/>
</EthernetPort>
<TdmModule>
  <TdmDisabledFrameSrcValue="0"/>
  <FramePolarity Value=""/>
  <FrameSamplingMode Value=""/>
  <DataSamplingMode Value=""/>
  <FromTdmTsstBufferSizeMs Value=""/>
  <ToTdmTsstBufferSizeMs Value=""/>
</TdmModule>
```
There are configuration parameters that should be customized with respect to their application. An example is given below:

```
<MaxNumTerm Value="800"/>
<MaxNumEchoTerm Value="400"/>
<MaxNumConferenceParticipants Value="128"/>
<MaxNumVideoRxQcif Value="32"/>
<MaxNumVideoRxCif Value="4"/>
<MaxNumVideoRxSd Value="1"/>
<MaxNumVideoRx720p Value="0"/>
<MaxNumVideoRx1080p Value="0"/>
<MaxNumVideoBufferQcif Value="224"/>
```

**NOTICE**

octvc1._config.arg file is provided as an example for 12dsp audio application. Align the resources of the DSP based on your application.

Also, keep the hardware-specific configuration parameters (port interface, TdmModule) as specified in the RPM. See the first set of configuration parameters above).

For details about setting the configuration parameters, see Octasic documentation *Vocallo Media Gateway API Configuration Guide*, and the `octvoctn5009-sys_config.pdf` file at `/opt/octasic/software/octvoc` location.

For details about using the firmware image generator, see Octasic documentation and the `oct2200m_boot_image_gen.html` file at `/opt/octasic/application/oct2200/oct2200_boot_img_gen` location.

Once you have created a new firmware image you should copy it to the `tftpboot` folder. For details about how to copy firmware image to the `tftpboot` folder, see *Executing Demo on page 47*. 
To load the new firmware image into the DSPs, execute:

```
# octservice stop all
# octservice start all
```

### 5.3.2 12xDSP Audio Transcode Demo

- An example application in source code and as an executable for the reference platform is provided in `12dsp_audio_transcode_net_api`.
- Details about using the demo, are provided in `README_max_channel_tests.txt`.

Both the executable and demo details are found here:

```
/opt/octasic/application/sample/octvoc/12dsp_audio_transcode_net_api
```
PCIE-8120 External Connectors

A.1 Overview

This appendix describes the pin assignments and signals for the connectors on the SharpMedia™ PCIE-8120 card.

The following figure shows the top and bottom view layout of the PCIE-8120.

*Figure A-1 PCIE-8120 Primary and Secondary Layout*
### A.2 SharpMedia PCIE-8120 Card Edge Connector

The following table provides pin assignment for the PCIE-8120 card edge connector.

Table A-1  SharpMedia PCIE-8120 Card Edge Connector Pin out

<table>
<thead>
<tr>
<th>Pin#</th>
<th>Name</th>
<th>Side B Description</th>
<th>Name</th>
<th>Side A Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+12V</td>
<td>12V power</td>
<td>PRSNT1 #</td>
<td>Hot-Plug presence detect</td>
</tr>
<tr>
<td>2</td>
<td>+12V</td>
<td>12V power</td>
<td>+12V</td>
<td>12V power</td>
</tr>
<tr>
<td>3</td>
<td>+12V</td>
<td>12V power</td>
<td>+12V</td>
<td>12V power</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>Ground</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>5</td>
<td>SMCLK</td>
<td>SMBus (System management Bus) clock</td>
<td>JTAG2</td>
<td>TCK (Test Clock), clock input for JTAG interface</td>
</tr>
<tr>
<td>6</td>
<td>SMDAT</td>
<td>SMBus System management Bus) data</td>
<td>JTAG3</td>
<td>TDI (Test Data Input)</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>Ground</td>
<td>JTAG4</td>
<td>TDO (Test Data Output)</td>
</tr>
<tr>
<td>8</td>
<td>+3.3V</td>
<td>3.3V power</td>
<td>JTAG5</td>
<td>TMS (Test Mode Select)</td>
</tr>
<tr>
<td>9</td>
<td>JTAG1</td>
<td>TRST# (Test Reset) resets the JTAG interface</td>
<td>+3.3V</td>
<td>3.3V power</td>
</tr>
<tr>
<td>10</td>
<td>3.3Vaux</td>
<td>3.3V auxiliary power</td>
<td>+3.3V</td>
<td>3.3V power</td>
</tr>
<tr>
<td>11</td>
<td>WAKE#</td>
<td>Signal for Link reactivation</td>
<td>PERST#</td>
<td>Fundamental reset</td>
</tr>
<tr>
<td>12</td>
<td>RSVD</td>
<td>Reserved</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>13</td>
<td>GND</td>
<td>Ground</td>
<td>REFCLK+</td>
<td>Reference clock (differential pair)</td>
</tr>
<tr>
<td>14</td>
<td>PETp0</td>
<td>Transmitter differential pair, Lane 0</td>
<td>REFCLK-</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>PETn0</td>
<td>GND</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>16</td>
<td>GND</td>
<td>Ground</td>
<td>PERp0</td>
<td>Receiver differential pair, Lane 0</td>
</tr>
<tr>
<td>17</td>
<td>PRSNT2 #</td>
<td>Hot-Plug presence detect</td>
<td>PERn0</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>GND</td>
<td>Ground</td>
<td>GND</td>
<td>Ground</td>
</tr>
</tbody>
</table>

**Mechanical Key**

<table>
<thead>
<tr>
<th>Pin#</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>RSVD</td>
<td>Reserved</td>
</tr>
<tr>
<td>13</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>14</td>
<td>PETp0</td>
<td>Transmitter differential pair, Lane 0</td>
</tr>
<tr>
<td>15</td>
<td>PETn0</td>
<td>GND</td>
</tr>
<tr>
<td>16</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>17</td>
<td>PRSNT2</td>
<td>Hot-Plug presence detect</td>
</tr>
<tr>
<td>18</td>
<td>GND</td>
<td>Ground</td>
</tr>
</tbody>
</table>
A.3 J1/J2 External Ethernet Connector Status LEDs (not available on -N versions)

Two 10/100/1000BASE-T IEEE802.3 compliant Ethernet ports are available on the PCIE-8120 via RJ-45 style connectors (except -N versions). They are provided through two transceiver devices (PHY) connected to the MSW.

- LED0: YELLOW: LINK
- LED1: GREEN: ACTIVE

Table A-1  SharpMedia PCIE-8120 Card Edge Connector Pin out (continued)

<table>
<thead>
<tr>
<th>Pin#</th>
<th>Name</th>
<th>Side B Description</th>
<th>Name</th>
<th>Side A Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>19</td>
<td>PETp1</td>
<td>Transmitter differential pair, Lane 1</td>
<td>RSVD</td>
<td>Reserved</td>
</tr>
<tr>
<td>20</td>
<td>PETn1</td>
<td></td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>21</td>
<td>GND</td>
<td>Ground</td>
<td>PERp1</td>
<td>Receiver differential pair, Lane 1</td>
</tr>
<tr>
<td>22</td>
<td>GND</td>
<td>Ground</td>
<td>PERn1</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>PETp2</td>
<td>Transmitter differential pair, Lane 2</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>24</td>
<td>PETn2</td>
<td></td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>25</td>
<td>GND</td>
<td>Ground</td>
<td>PERp2</td>
<td>Receiver differential pair, Lane 2</td>
</tr>
<tr>
<td>26</td>
<td>GND</td>
<td>Ground</td>
<td>PERn2</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>PETp3</td>
<td>Transmitter differential pair, Lane 3</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>28</td>
<td>PETn3</td>
<td></td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>29</td>
<td>GND</td>
<td>Ground</td>
<td>PERp3</td>
<td>Receiver differential pair, Lane 3</td>
</tr>
<tr>
<td>30</td>
<td>RSVD</td>
<td>Reserved</td>
<td>PERn3</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>PRSNT2#</td>
<td>Hot-Plug presence detect</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>32</td>
<td>GND</td>
<td>Ground</td>
<td>RSVD</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

End of the x1 connector

End of the x4 connector
PCIE-8120 External Connectors

A.4 P2 External ATX 6-pin Power Connector (only on -N versions)

An ATX 6-pin power connector is available at the P2 location for the NEBS optimized (-N) variants of the PCIE-8120 card. As under NEBS exceptional operation conditions, the current drawing from the slot connector could exceed the maximum allowed per pin current. The -N variants receive 12V supply power exclusively from the P2 connector.

For more details on the P2 connector, see PCI Express x16 Graphics 150W-ATX Specification document listed in Related Specifications on page 107.

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+12V</td>
</tr>
<tr>
<td>2</td>
<td>+12V</td>
</tr>
<tr>
<td>3</td>
<td>+12V</td>
</tr>
<tr>
<td>4</td>
<td>Ground</td>
</tr>
<tr>
<td>5</td>
<td>Sense</td>
</tr>
<tr>
<td>6</td>
<td>Ground</td>
</tr>
</tbody>
</table>

A.5 Debug Connectors

The PCIE-8120 card is equipped with several debug ports. The debug ports allow DSP/MFA,CPLD/FPGA programming, and JTAG/BSCAN functionality.

- P4201 serial port MFA: RS-232 style debug port for the MFA application
- P5001 OCT-SDBI2 debug port: The Octasic Pod requires an adapter cable for the micro-header
  - The connector style is a 16-pin, 1.27mm pitch micro-header

For more information, contact SMART Embedded Computing and refer to part number 30NL9302D24.

A.6 P3 Fan Unit Connector (optional component)

The PCIE-8120 card supports a heat sink assembly that is equipped with a fan or blower unit. A three-pin header provides 12V supply for this purpose. An additional buffer circuitry allows for PWM fan speed control via the CPLD.
Molex 3-pin header 53398-0371, pico-blade series.
- 12V /200 mA max. PWM drive capability for a 2.4W class fan/blower unit or high impedance 2k/20k PWM control input.

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>12V main supply (1A max.)</td>
</tr>
<tr>
<td>2</td>
<td>FAN_PWM_CTRL (3.3V logic level PWM control or 12V/200 mA PWM driver)</td>
</tr>
<tr>
<td>3</td>
<td>GND main supply</td>
</tr>
</tbody>
</table>
PCIE-8120 Hardware Description

B.1 Overview

This section describes the key hardware components of the SharpMedia PCIE-8120 card.

B.2 PCIE-8120 Card Block Diagrams

The following figures provide an overview of the main function blocks of the PCIE-8120 and how they are interconnected.

Figure B-1 Card Block Diagram SharpMedia PCIE-8120-A12/V12
Figure B-2  Card Block Diagram SharpMedia PCIE-8120-A04
Figure B-3  Card Block Diagram SharpMedia PCIE-8120-A/V12-N/-N-PP
B.3 Card Reset Architecture

The following figure provides an overview of PCIE-8120 card reset architecture.

Figure B-4 Card Reset Diagram

All devices on the card that provide a dedicated reset input are connected to the CPLD to allow for individual reset control at start up or during runtime via host control. The PERST_N signal is propagated to the Ethernet network devices (NIC, Switch, PHY) to make the card behave like a standard NIC card. All other functions are kept in reset state and released only on S/W driver activity to allow for correct set up before going active, for example, Switch/PHY configuration, MFA startup, DSP boot loading.

B.4 Power Supply Architecture

The following figure provides an overview of the power supply architecture of PCIE-8120.

**Figure B-5  Board Power Supply Architecture**

The PCIE-8120 uses seven DC/DC building blocks to provide the necessary operating voltages that are required by the devices on the board.

- Main voltage supply comes from the 12V card edge or ATX 6-pin connector via the assembly option. For more information, see *P2 External ATX 6-pin Power Connector (only on -N versions)* on page 60.
- 3.3V from card edge supplies power-up control circuitry
- 3.3V aux is not used (no wake capability)
- Current/voltage/power monitor, see *I/V/P Sensors on page 77*
- Card power management control by CPLD, see *Card Power Management on page 73*

According to the *PCI Express Card Electromechanical Specification Rev.2.0.2007.PCISIG CEM 2.04/11/2007*, the PERST# signal indicates a system power good status combined with a card reset function. Therefore, it cannot be used as a power good signal to the cards power-up control for the local DC/DC units. To keep up with the timing requirements for the PERST# signal, the local power control must enable the DC/DC units immediately after card edge power appears. An under-voltage lockout circuitry is used to provide a status signal that indicates when the 12V main supply is within the allowed range:

- DC/DC enable for VP12 > 11.08V (calculated)
- DC/DC disable for VP12 < 8.5V (calculated)
B.5  Card Clock Architecture

The following figure provides an overview of the card clock architecture of PCIE-8120.

Figure B-6  Card Clock Scheme

A synchronous clocking scheme is used for the DSP building blocks to allow for task distribution over several DSPs. All other components have individual clocking sources.

- Oscillators are EPSON SG-210 or equivalent types, +/-50ppm tolerance
- Resonators are EPSON FA238 or equivalent types, +/-23ppm tolerance
- Clock buffer device is TI CDCLVC1112

B.6  Ethernet NIC

The PCIE-8120 card uses an Intel 82580EB/DB Gigabit Ethernet Controller to implement PCI Express connectivity and thereby provides access for the host system towards the card’s resources. This device supports up to four Ethernet ports with integrated MAC units and SGMII/SerDes interface. The ports are connected to the Ethernet switch unit on the card. Also, see Ethernet Port Mappings on page 70. The host interface supports a PCI Express v2.0 x4, x2, x1 link with 5 Gbps and 2.5 Gbps operation.
B.6.1 NV-Memory-NIC Configuration

The PCIE-8120 card stores configuration data for the Intel i82580EB/DB device on a local EEPROM device. The configuration data for individual variants is according to port mapping. See, Ethernet Port Mappings on page 70.

- MAC Addresses: factory programmed
- Subsystem Vendor ID set to 0X1223 for SMART EC
- Subsystem ID set to 0x0016

B.7 Ethernet Switch Unit

Based on the variant PCIE-8120 uses one or two 16-port SerDes Gigabit Ethernet switch devices to allow full bandwidth connectivity between all on board resources.

- Broadcom BCM5396 device, 256-pin FBGA package
- 16-port 10/100/1000 Mbps integrated switch controller

B.7.1 Main Switch Unit (MSW) - BCM5396

The main switch unit (MSW) is available on all versions of the PCIE-8120 card and provides the basic connection between all DSP, NIC, MFA, and external Ethernet resources.

B.7.2 Video Switch Unit (VSW) - BCM5396

The Video Switch Unit (VSW) is available on variants that provide additional network connection between DSP, NIC, MFA, and external Ethernet resources. The main task of the VSW is to connect the second Ethernet port of the DSP units to the switch fabric.
B.7.3 Ethernet Port Mappings

The following figures show the port mappings of the Ethernet fabric on the individual variants of the PCIE-8120 card.

*Figure B-7 Port Mapping PCIE-8120-A12/V12*
Figure B-8 Port Mapping PCIE-8120-A04
B.8 Media Flow Aggregator (MFA) Unit

The PCIE-8120 card is optionally equipped with an Octasic OCT1503 MFA FPGA. The purpose of the device is to aggregate an array of Ethernet devices (i.e., the OCT2224 DSP array) to form a single logical node. For more information on Octasic OCT1503 MFA FPGA, see OCT1503 MFA FPGA Specifications. 2012. OCT1503DS9000 listed in Related Specifications on page 107.

The MFA provides following features:

- FPGA design based on Altera EP3C25F256 device (Cyclone III Family)
- Field update programming through Ethernet API
- Interfaces: 2x GMII via MFA PHY 1 & 2 connected to VSW (default) or MSW based on assembly option
  - Interface MFA#1 used as device port (DSP side)
  - Interface MFA#2 used as aggregated port (network and control processor)
- Serial debug port option (RS-232) via 3-pin header P4201
B.9 Glue Logic - CPLD

The PCIE-8120 card is equipped with a CPLD to support additional functionality that is required by the design but not provided by the main components selected for the card. The functional details are as follows:

- Lattice MachXO2-1200U, -4 device, 256-ball caBGA
- Single 3.3V supply from card edge connector
- Internal 20MHz clock and power-up watchdog
- Internal UFM stores hardware settings and product-specific information
- Optional external flash for persistent storage of user configuration data
  - AT25256 device, 256 kbits density, 8S1 SOIC package

B.9.1 Card Power Management

The CPLD on the PCIE-8120 fulfills the functionality of a power management controller for the card. The power-up and power-down control is based on the input signals.

- Internal power good status, that is, 3.3V from PCIE slot is present and the device has started properly
- VP12_FAIL signal indicating when the 12V main supply is not within the allowed range
- PERST# signal from PCIE connector indicating the system preparing to go into operation or leaving operational mode
- VPx_PWRGD status signals of the on board DC/DC units

Based on the status of the input signals, the following control signals display output:

- VPx_PWREN enables/disables the DC/DC units according to power-up/down timing sequence requirements
  - Default power-up/down sequence is simultaneous
- PWRDN_VP discharges the residual voltage levels after powering off the DC/DC units
B.9.2 Interfaces and Software Control

B.9.2.1 MDIO

The MDIO[1] channel from the second SerDes port of the NIC is connected to the CPLD for basic software access via mapped pseudo-PHY registers. A card-specific enhanced network card driver is necessary to make use of the functionality that is provided through the CPLD. For more information on interfaces and software control, see SharpMedia PCIE-8120 Software Package on page 36.

B.9.2.2 Card Variant MOD_ID

The card provides a 4-bit wide H/W strapped ID (MOD_ID<3..0>). It is used to identify the variant of the card. Based on the variant, some settings in the CPLD are different or specific registers are not available.

The OS device driver or user mode S/W can make use of the MOD_ID to make user-specific settings or specific functions available for the respective card.

Table B-1  Card Variant MOD_ID

<table>
<thead>
<tr>
<th>Order Number</th>
<th>MOD_ID&lt;3...0&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCIE-8120-A12</td>
<td>0111</td>
</tr>
<tr>
<td>PCIE-8120-V12</td>
<td>0111</td>
</tr>
<tr>
<td>PCIE-8120-A04</td>
<td>0100</td>
</tr>
<tr>
<td>PCIE-8120-V04</td>
<td>0100</td>
</tr>
<tr>
<td>PCIE-8120-A12-N</td>
<td>0011</td>
</tr>
<tr>
<td>PCIE-8120-V12-N</td>
<td>0011</td>
</tr>
<tr>
<td>PCIE-8120-A12-N-PP</td>
<td>0010</td>
</tr>
<tr>
<td>PCIE-8120-V12-N-PP</td>
<td>0010</td>
</tr>
</tbody>
</table>

B.9.2.3 Card BASE_ID

The card provides a 4-bit address register for the DSP array (BASE_ID<3...0>). It is used to differentiate multiple cards within a system from the software point of view. It can be used to store the IP address range of a card in the UFM or to reconfigure an exchanged card to respond to the same IP address range than the original card.

The default value for BASE_ID<3..0> is 0b1111.
B.9.2.4 Opus Debug Port Multiplexer

The CPLD contains multiplex logic to select an individual DSP unit for debugging. The signals from the OCT-SBDI2 Pod connection header are routed to the CPLD and the CPLD has a set of SBDI output signals to every of the twelve DSP units. For more information on how to set up OCT-SBDI2 debug connection, refer to OCT2200UG8002 User Guide listed in Related Specifications on page 107. Also, refer to OPUS Debug Port on page 83.

B.9.2.5 SMBus and PVT_I2C Bus

The PCIE-8120 card provides connectivity to the PCI Express connector SMBus. Additionally, a private I2C bus (PVT_I2C) is available that accesses the on-board sensor devices. Both are connected to the CPLD to allow access to the sensor information via SMBus or through the host system via MDIO.

The CPLD is connected as a slave device on the PCI Express SMBus.

*Figure B-10 SMBus and PVT_I2C bus connection diagram*

ID PROM (optional)

A serial EEPROM is available on the PVT_I2C bus for the purpose of storing manufacturer or user data specific to the card. This ID PROM device is optional and may not be present on specific variants of the card.

- M24C04 Device
- 4 kbits density
- I2C address: 0xA0
- Temperature sensors
PCIE-8120 Hardware Description

There are two temperature sensors on the PVT_I2C bus for monitoring the temperature on the card and the thermal behavior of the system. One sensor is placed on the mounting bracket side which is considered as the air outlet side. The other sensor is placed on the card retainer side which is considered as the air inlet side, see Temperature Sensor Location on page 76.

These sensors measure the PCB component temperature, which allows for the determination of absolute and delta temperature levels on the card. A possible sensor fault or a cooling system degradation can also be indicated.

**NOTICE**

The PCB component temperature may not be very closely correlated to the system or card ambient temperature as specified in Environmental and Thermal Requirements on page 32. The PCB component temperature is largely dependent on specific mechanical and thermal conditions in the respective server where the card is installed. See, Sensor alert default values on page 78.

- Sensor type is a LM75 device
- I2C address: 0x90 for air inlet temperature sensor
- I2C address: 0x92 for air outlet temperature sensor

An additional temperature sensor is available at the SMBus in conjunction with the NIC device. It allows monitoring the temperature of the device.

- ADT7461 Device
- SMB address 0x4C

*Figure B-11 Temperature Sensor Location*
I/V/P Sensors

A current and power monitor device is available on the PVT_I2C bus for surveillance purpose. It monitors the 12V bus power and can be used to control the card’s power consumption or provide alerts about over-current or under-voltage that can be handled via the CPLD interface.

- INA226 Device
- I2C address: 0x88
- Programmable alerts for
  - Power
  - Current
  - Voltage
- Alert_INT to CPLD

Check the power consumption of the card with the command. An example is given below:

```
# PCIE-8120-read-sensor

PCIE-8120#0:
  t_inlet: 31°C
  t_outlet: 32.5°C
  ivp_volt: 11.9425V
  ivp_curr: 1.84125A
  ivp_powr: 17.575W
```

Sensor Alert Default Values

Until the PCIE-8120 is fully characterized in a reference system environment, system integrators can use values to set up sensor alarms.

It is proposed to use a smart sensor algorithm that collects data from the sensors, verifies readings and calculates history, acts quickly on critical levels, and still does not overload the low bandwidth of the interface. It should be noted that these types of sensors are not useful for transient alarms, for example short voltage dips or current peaks.

A three-level approach to sensor alarms seems appropriate with the following strategy:

- Minor: Readings in this range should be tracked (response time: minutes)
- Major: Actions to reduce load should be taken/requested (response time: less than a minute)
PCIE-8120 Hardware Description

- Critical: Emergency shutdown/store event to NVRAM (response time: few seconds)

Following are the values to set up sensor alarms:

**Table B-2  Sensor alert default values**

<table>
<thead>
<tr>
<th>Sensor type</th>
<th>Minor</th>
<th>Major</th>
<th>Critical</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inlet Temp</td>
<td>&gt;50°C</td>
<td>&gt;55°C</td>
<td>&gt;60°C</td>
</tr>
<tr>
<td>Outlet Temp</td>
<td>&gt;55°C</td>
<td>&gt;70°C</td>
<td>&gt;80°C ***</td>
</tr>
<tr>
<td>Delta Temp</td>
<td>&lt;5°C *</td>
<td>&gt;15°C</td>
<td>&gt; 0°C</td>
</tr>
<tr>
<td>Card Power 12 OCT</td>
<td>60W@12V</td>
<td>65W@12V</td>
<td>70W@12V</td>
</tr>
<tr>
<td>Supply Bus voltage</td>
<td>&lt; 11.5V</td>
<td>&lt; 10V</td>
<td>&lt; 9V</td>
</tr>
<tr>
<td>Supply Bus current 4 OCT</td>
<td>1.8A **</td>
<td>2.1A **</td>
<td>2.5A **</td>
</tr>
<tr>
<td>Supply Bus current 12 OCT</td>
<td>&gt;5 Amp</td>
<td>&gt;6.5 Amp</td>
<td>&gt;7 Amp</td>
</tr>
<tr>
<td>Card Power 4 OCT</td>
<td>22W@12V</td>
<td>26W@12V</td>
<td>30W@12V</td>
</tr>
<tr>
<td>Card Power 12 OCT -N****</td>
<td>60W@12V</td>
<td>78W@12V</td>
<td>84W@12V</td>
</tr>
<tr>
<td>Card Power 12 OCT -N-PP*****</td>
<td>55W@12V</td>
<td>60W@12V</td>
<td>65W@12V</td>
</tr>
</tbody>
</table>

* A low delta temperature reflects poor system cooling capability.
** It is not recommended to use current readings for alarms as they depend on varying voltage. Use card power readings instead.
*** The PCIE-8120 temperature sensors are preconfigured to shutdown the card when either sensors reach 80°C. The system can restart when the temperature falls below 75°C.
**** The higher sensor readings for -N version reflect exceptional operating conditions per NEBS requirement.
***** 66W@ 12V is the maximum allowed power continually drawn from the PCIe slot connector.

**B.9.2.6  Debug LED**

The PCIE-8120 provides eight debug LEDs to the CPLD to indicate the power-up status and generic fault conditions. The LEDs 0-7 are located on the top component side of the card near the PCI Express connector, oriented from left to right. In default run state, all LEDs are off. For LED error codes see the table below:

**Table B-3  LED Error Code (For 0, 1 and 2)**

<table>
<thead>
<tr>
<th>LED NUMBER</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 1 0</td>
<td>Enable state-12V stable</td>
</tr>
</tbody>
</table>
B.9.3 CPLD Upgrade

The CPLD offers the capability to reprogram its configuration data under host software control. The procedure is not fail safe status. This means, if a reprogramming procedure fails, the whole card becomes unusable and needs to be reprogrammed via hardware (download cable).

CPLD can be upgraded by using the following procedure:

1. Boot the OS with PCIE-8120 drivers installed and new CPLD image available.

### Table B-3  LED Error Code (For 0, 1 and 2)

<table>
<thead>
<tr>
<th>LED NUMBER</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 1 0</td>
<td></td>
</tr>
<tr>
<td>Off Off On</td>
<td>Enable state-on-board converters enabled</td>
</tr>
<tr>
<td>Off On Off</td>
<td>Wait state-Power good status</td>
</tr>
<tr>
<td>Off On On</td>
<td>Wait state-Power-up sequencing</td>
</tr>
<tr>
<td>On Off Off</td>
<td>Power good status and PERST_N deasserted</td>
</tr>
<tr>
<td>On Off On</td>
<td>N/A (shutdown)</td>
</tr>
</tbody>
</table>

### Table B-4  LED Error Code (For 3, 4, 5,6 and 7)

<table>
<thead>
<tr>
<th>LED NUMBER</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 6 5 4 3</td>
<td></td>
</tr>
<tr>
<td>Off Off Off Off Off Off</td>
<td>No Error</td>
</tr>
<tr>
<td>Off Off Off Off Off On</td>
<td>12V Failed</td>
</tr>
<tr>
<td>Off Off Off Off On Off</td>
<td>3.3V Failed</td>
</tr>
<tr>
<td>Off Off Off On Off On</td>
<td>2.5V Failed</td>
</tr>
<tr>
<td>X X On Off Off</td>
<td>1.5V Failed (additional 1.2V or 1.0V)</td>
</tr>
<tr>
<td>X On X Off Off</td>
<td>1.2V Failed (additional 1.5V or 1.0V)</td>
</tr>
<tr>
<td>On X X Off Off</td>
<td>1.0 V Failed (additional 1.5V or 1.2V)</td>
</tr>
<tr>
<td>Off Off On Off On</td>
<td>PERST_N deasserted before power good status</td>
</tr>
<tr>
<td>Off On Off Off On</td>
<td>Not all power good status within timeout</td>
</tr>
</tbody>
</table>
PCIE-8120 Hardware Description

2. Initialize the card by using the command:

   /opt/bladeservices/bin/pcie8120-init

3. Erase the old CPLD image by using the command.

   /opt/bladeservices/bin/pcie8120-tool --dev=cpldx -- flasherase=cfg

4. Program the CPLD with new firmware image.

   /opt/bladeservices/bin/pcie8120-tool --dev=cpldx -- flashwrite=cfg 0 <file_new_cpld_fw_image>

5. Power cycle the board.

B.10 DSP Array

The PCIE-8120 DSP array can be populated with up to 12 instances of Octasic’s DSP OCT2224M System-On-Chip device, which is specialized for media gateway applications. For more information on the Octasic DSP OCT2224M, refer to the OCT2200M Hardware Specification listed in Related Specifications on page 107.

The following sections describe specific aspects of the PCIE-8120 design.

B.10.1 DSP Overview

The Octasic OCT2224M DSP is part of the OCT2200 series of devices which is a family of Digital Signal Processors (DSP) based on the Opus 2 architecture developed by Octasic. It is targeting voice and video applications for telephony infrastructure applications.

The OCT2224M is composed of five major subsystems:

- The Opus2 DSP subsystem
- The DDR memory subsystem
- The high-speed I/O subsystem (Ethernet MAC Engines)
- The resources subsystem (GPIO)
- The maintenance subsystem (Boot Controller)

The main features of the OCT2224M are:

- 24 Opus2 cores with 144k bytes of L1 memory per core
- C programmable DSP
- 484-pin BGA 1.0 mm pitch
- 4W typical power consumption
PCIE-8120 Hardware Description

- Secure custom booting capability
- Precision clock synchronization on external references
- Various peripheral interfaces Ethernet, serial/parallel hi-speed interfaces, TDM, flash, etc. For details, see document OCT2200MDS8000 listed in Related Specifications on page 107.

B.10.2 DDR3 Memory Subsystem

The 32-bit DDR memory controller is used for interface to JEDEC DDR3 SDRAM devices. The interface supports 4.32GB/s at a 1080MHz data rate (540MHz clock rate).

The DSP memory on the PCIE-8120 is realized with two DDR3 x16 devices per DSP. The memory access is 32-bits wide.

The default memory size is 512 MByte.

The DDR3 memory is not used until the DDR configuration is obtained from the boot image.

B.10.3 Ethernet MAC Engines

The OCT2224M device on the PCIE-8120 card configures two Ethernet MAC engines, supporting 10/100/1000-Mbps data transfer rates on the physical interfaces: SERDES2 and SERDES3 in SGMII mode. See Table B-5 below.

EMAC0 and EMAC2 support jumbo packets (maximum size of 9,018 bytes or 9,022 bytes for VLAN frames). EMAC2 is available for BOOTP.

Table B-5  Ethernet Physical Interface Mapping

<table>
<thead>
<tr>
<th>Mode</th>
<th>SERDES0</th>
<th>SERDES1</th>
<th>SERDES2</th>
<th>SERDES3</th>
<th>Eth0</th>
<th>Eth1</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>EMAC 1 (not used)</td>
<td>EMAC 3 (not used)</td>
<td>EMAC 2</td>
<td>EMAC 0</td>
<td>n/a</td>
<td>n/a</td>
</tr>
</tbody>
</table>

B.10.4 Boot Controller

The boot controller is responsible for managing the boot process. The boot process loads a boot image that is created by an Octasic software tool that allows the user to specify optional device configuration and the application image to load.

The boot process uses a default device configuration determined by a lowest common capability and/or the BOOT_MODE to load a boot image. The final device configuration information is obtained from the boot image and can override the one used for the boot process.
The SharpMedia PCIE-8120 card is configured for BOOTP on EMAC 2 on SERDES 2 (SGMII, 1Gbps).

**B.10.5 DSP Configuration**

The following table lists the assignment of the DSP control and configuration pins:

*Table B-6 DSP Control Signals*

<table>
<thead>
<tr>
<th>Signal Group</th>
<th>Controlled by</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSPx_RST_N</td>
<td>CPLD</td>
<td>Reset input to each DSP</td>
</tr>
<tr>
<td>DSPx_INT_N</td>
<td>CPLD</td>
<td>Interrupt output from each DSP</td>
</tr>
<tr>
<td>DSPx_USER_HW_CONF[3:0]</td>
<td>HW Strapping</td>
<td>DSP position on mezzanine set by strapping resistors range 0 - 11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0000 = DSP0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0001 = DSP1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0010 = DSP2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0011 = DSP3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0100 = DSP4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0101 = DSP5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0110 = DSP6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0111 = DSP7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1000 = DSP8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1001 = DSP9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1010 = DSP10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1011 = DSP11</td>
</tr>
<tr>
<td>DSPx_USER_HW_CONF[7:4]</td>
<td>BASE_ID[3:0]</td>
<td>A card-specific 4-bit Base ID can be programmed via the CPLD</td>
</tr>
<tr>
<td>DSPx_USER_HW_CONF[13:8]</td>
<td></td>
<td>Strapped by resistor to 1</td>
</tr>
<tr>
<td>DSPx_USER_HW_CONF[14]</td>
<td>CPLD</td>
<td>0 = Unique factory-burned per-chip MAC address</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = TFTP server with IP derived from 00:0C:90:02:&lt;USER_HW_CONFIG&gt;xx</td>
</tr>
<tr>
<td>DSPx_USER_HW_CONF[15]</td>
<td>CPLD</td>
<td>0 = TFTP server at 192.168.1.200</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = TFTP server with IP derived from 192.168.&lt;USER_HW_CONFIG&gt;xx</td>
</tr>
<tr>
<td>BOOT_MODE[3:0]</td>
<td>HW Strapping</td>
<td>Strapped by resistor to</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0100 = BOOTP on EMAC 2 on SERDES 2</td>
</tr>
</tbody>
</table>
B.10.6 DSP 25MHz Clock Synchronization

The PCIE-8120 card provides clock synchronization for the entire DSP array to make sure of equal processing time on computing tasks that are shared between two or more DSP units. The synchronized main DSP operating clock is 25MHz.

B.10.7 OPUS Debug Port

A debug port is available for low level debugging of individual DSP units via the vendor specific Opus Studio development suite.

- Opus debug port via connector P5001
- 16-pin 1.27 mm pitch micro header
- DSP debug port selection via CPLD
PCIE-8120 Hardware Description
Appendix C

Known Issues

C.1 OctSetup Known Issues

1. When starting octSetup for the first time you might observe the following message.

   SELINUX: labeling directory /var/lib/tftpboot with tftpdir _rw_t ...libsemanage.dbase_llist_query: could not query record value (No such file or directory)

   This message can be ignored. It has no impact on the correct functionality of octSetup. This is a known issue of the tool semanage, which is called by octSetup.

2. When executing octSetup the following messages are displayed.

   Note: Optional package xxx not installed

   This message is a hint and can be ignored as long as you plan only to start the demo. If you plan to do some development for the DSPs, you should consider installing the optional package indicated by the following message.

   Error: mandatory package xxx not installed

   If you get this message, then you should install the missing package and execute octSetup again. Install a missing package with:
   # yum install xxx

C.2 DSP Known Issues

When there is no connection between host and DSP, the following error is displayed instead of the error statistics.

1. Error:

   cOCTVC1_VSPMP_VOC_MSG_MODULE_GET_CONFIG failed, rc = 0x0a0a0003
   (cOCTVC1_PKT_API_RC_TIMEOUT)

   ulNumConnections out of range : 0

2. If every DSP displays:

   ulNumConnections out of range : 0

   Check that the SMART Embedded Computing License file is included.
D.1 OctSetup: Internal Behavior

OctSetup sets up the host for the demo. The following figure illustrates the network setup of the host.

Figure D-1 Host Network Setup

NOTICE

MSW and VSW are identical from functional point of view. They route the two links of a DSP to the host.

CPLD is used for board management and control and has no access to the DSPs.
At boot time, the numbering of the network devices of the card is completed. This numbering is arbitrary and differs from system to system. Use ethx, ethy and ethz as placeholders in the above example set up.

No network device is connected to ethy. The pseudo device ethy is only to access the CPLD. Avoid finding a link at this device and configuring an IP-address used to access.

It is not required to define an IP address for the network devices ethx and ethz. The DSPs use a MAC-based protocol and not an IP-based protocol. However, you can identify the MAC address of the network device and configure the IP address for these devices.

The default VLAN ID of the DSP ports at MSW is 999. It indicates that the switch adds the VLAN tag with ID 999 for every untagged packet received at a port.

**NOTICE**

When you develop an application running on the DSPs, you can define your own VLAN for your application packets or remove/disable VLAN 999 after the DSPs have loaded its firmware image. You can select any other ID except zero to develop the application after the DSPs have loaded their firmware images.

When the DSP requests an IP address from the DHCP server, the server selects an arbitrary IP-address from the range 192.168.100.[10-21]. There is no fixed relation between IP-address and DSP number. Additionally, there is no need to prefer this particular subnet 192.168.100.0. You can select any subnet.

- If a second card is installed in the system, the subnet for that card is 192.168.101.0. The system that octSetup uses is 192.168.[100 + card#].0. You can select any system or subnet.
- The configuration files for the DHCP server are in the /opt/bladeservices/etc directory. The DHCP configuration file name is pdevn-dhcpd.conf.
- The switch VSW is also used for internal data/packet exchange between the DSPs.

Place the DSP firmware images in the root directory of the TFTP server (or a subdirectory of TFTP server). The default is /var/lib/tftplib directory.

OctSetup creates pcie1820(pdevn directories in the TFTP root directory. Where n is the PCI-bus number of the card. Therefore, find a pdevn directory for every card in the host.

**NOTE:** For information on how to find a PCI bus number, see the section Identifying Cards on the PCI-Bus on page 89.
octSetup creates links for the boot files of the DSPs in the pdevn directories. The identification is oct2200.0 for DSP0 of the card, oct2200.1 for DSP1 of the card and so on. These boot files are links to the firmware image that should be loaded to the respective DSP. You can change the links to point to different boot files. Similarly, you can load an individual firmware image into every DSP. The identification system is set up in the configuration files of the DHCP server pdevn-dhcpd.conf in /opt/bladeservices/etc.

If you have to reload the firmware image, first put DSP in reset and then take it out of reset again. The DSP starts to load a firmware image. Use the octmezz tool with -- dspctrl=[up|down] option to perform these steps.

D.2 Identifying Cards on the PCI-Bus

Use pcie8120-listdev tool to identify all cards in the system on the PCIe bus.

Below is the sample output:

```
# pcie8120-listdev
PCIE-8120-A12/V12#0
  MSW0: 01:00.0 eth29
  CPLD0: 01:00.1 eth31
  VSW0: 01:00.2 eth30

PCIE-8120-A12/V12#1
  MSW1: 05:00.0 eth6
  CPLD1: 05:00.1 eth7
  VSW1: 05:00.2 eth5
```

The second column shows the PCI device of the function of a card. For example, MSW0 is at 01:00.0, which is bus 1, slot 0, function 0. You can identify this in the output of the tool lspci.

```
# lspci
00:00.0 Host bridge: Intel Corporation 2nd Generation Core Processor Family DRAM Controller (rev 09)
...
```
01:00.0 Ethernet controller: Intel Corporation 82580 Gigabit Backplane Connection (rev 01)

01:00.1 Ethernet controller: Intel Corporation 82580 Gigabit Backplane Connection (rev 01)

01:00.2 Ethernet controller: Intel Corporation 82580 Gigabit Backplane Connection (rev 01)

...

05:00.0 Ethernet controller: Intel Corporation 82580 Gigabit Backplane Connection (rev 01)

05:00.1 Ethernet controller: Intel Corporation 82580 Gigabit Backplane Connection (rev 01)

05:00.2 Ethernet controller: Intel Corporation 82580 Gigabit Backplane Connection (rev 01)

...

D.3 Card Serial Number

Use the `pcie8120-serialno` tool to determine the serial number of all cards installed in the system.

The sample output below shows the serial number of the cards zero and one:

```
# pcie8120-serialno
PCIE-8120#0: 6010687046XX
PCIE-8120#1: 601068703YXX
```

D.4 Switches Flow Control

By default, the flow control between all switch ports connected to the DSPs on PCIE-8120 cards are not enabled when PCIE-8120 card is initialized using the `pcie8120_init` command. Due to errata of the switch chip used on PCIE-8120 cards, the flow control cannot be set on all the ports individually, but it can be set on certain pairs of ports as given below:

- \((0, 10), (1, 11), (2, 12), (3, 13), (4, 14), (5, 15), (6, 16)\).
BCM5396 switch chips has 17 ports. Out of 17 ports:

- 16 ports (port #0 through #15) are connected on PCIE-8120 to either DSPs or front panel RJ-45 connectors, or to the host interface
- Port#16 is a special purpose port and is not connected on PCIE-8120

Flow control on ports 7, 8 and 9 can be set individually. Flow control on port 11, 12 and 15 connected to DSPs is not enabled by default, due to the above errata.

The following commands would enable flow control for ports 1 and 11, 2 and 12 and 5 and 15. For example,

```
# octmezz --dev=msw0 -w 0x00 0x61 0xbb
msw0: PG:REG 0x0:0x61 -> 0x00bb

# octmezz --dev=msw0 -w 0x00 0x62 0xbb
msw0: PG:REG 0x0:0x62 -> 0x00bb

# octmezz --dev=msw0 -w 0x00 0x65 0xbb
msw0: PG:REG 0x0:0x65 -> 0x00bb
```

D.5 Verify Flow Control

For a particular port, we can verify if flow control is enabled or disabled by reading

- TX PAUSE status register (Page 0x01, addr 0x14 - 0x17), and
- RX PAUSE status registers (page 0x01, addr 0x18)

Command to read TX PAUSE Status registers

```
#octmezz --dev=msw0 -r 0x01 0x14
```

Command to read RX PAUSE status register

```
#octmezz --dev=msw0 -r 0x01 0x18
```

TX PAUSE and RX PAUSE status registers are the bit fields indicating the status for each 10/100/1000BASE-T ports. bit0 -> port0 and bit15-->port15.
D.6 Disable Flow Control

To disable flow control, a value of 0x8b needs to be written to the register at page 0x01 and reg address 0x60 - 0x6F based on port number.

Sample commands to disable flow control on ports1 and 2

#octmezz --dev=msw0 -w 0x01 0x61 0x8b (disable flow control on port1)
#octmezz --dev=msw0 -w 0x01 0x62 0x8b (disable flow control on port2)

D.7 12xDSP Audio Transcode VoIP Channel Demo Application

The following is additional information available at this location:

README_max_channel_tests.txt file at
/opt/octasic/application/sample/octvoc/12dsp_audio_transcode_net_api

Figure D-2  Block Diagram

12dsp_audio_transcode_net_api - sets up to 400 IP-to-IP channels (800 IP end points) per DSP. The main purpose of this software is to load the DSPs with maximum IP-to-IP channels so that the test is set in pairs of physical DSPs.

This software code assumes that there are 12 DSPs available and that the code is running on the Xeon server host with RHEL, though it should run on other hosts.

NOTE: Main change is to change the data structures to large arrays.

Some functions are copied from existing sample files and are named as MyXXXXXXX, whereas xxxxxxxx is the original function name.
DSP IP Addresses are controlled by these #defines

```c
#define DSP_IP_BASE 0xC0A84C00
#define DSP_IP_START 201
#define DSP_IP_FINISH (DSP_IP_START+MAX_DSPS-1)
```

So, with current settings these IP addresses are used:

DSP0 IP : 192.168.76.201
DSP11 IP : 192.168.76.212

### D.7.1 Requirements

The following requirements must be fulfilled to enable the demo application to run:

- This demo application is compiled with Octasic SDK version 1.9.3
- The DSP image must have the SMART Embedded Computing specific license file included. This means the DSPs must be out of reset and the image downloaded via TFTP.
- The IP address is not important because the software uses raw sockets to communicate with the DSPs

### D.7.2 Running Software

#### D.7.2.1 New features

If any of these counters are non-zero, a warning is displayed at the end of each output of the DSPs statistics list.

- `ulRxBadPktTypeCnt`
- `ulRxBadRtpPayloadTypeCnt`
- `ulRxBadPktHdrFormatCnt`
- `ulRxBadPktLengthCnt`
- `ulRxMisorderedPktCnt`
- `ulRxLostPktCnt`
- `ulRxBadPktChecksumCnt`
- `ulRxUnderrunSlipCnt`
- `ulRxOverrunSlipCnt`
- `ulRxVocoderChangeCnt`
- `ulRxCircularBufferWriteErrCnt`
- `ulRxApiEventCnt`
### Miscellaneous

- `ulTxInBadPktPayloadCnt`
- `ulTxTimestampGapCnt`
- `ulTxTdmWriteErrCnt`
- `ulRxToneDetectedCnt`
- `ulRxToneRelayEventPktCnt`
- `ulRxToneRelayUnsupportedCnt`
- `ulTxToneRelayEventPktCnt`
- `ulTxApiEventCnt`
- `ulTxNoRtpEntryPktDropCnt`
- `ulConnectionWaitAckFlag`
- `ulRxMipsProtectionDropCnt`
- `ulTxMipsProtectionDropCnt`

The output below are the results when an error is detected:

```plaintext
--- VOC TERM MC STATISTICS (DSP 03) ------------------------------
   | RxOutPktCnt : 125190214
   | RxInSidPktCnt : 0
   | RxNoPktCnt : 1236800
   | RxBadPktTypeCnt : 0
   | RxBadRtpPayloadTypeCnt : 0
   | RxBadPktHdrFormatCnt : 0
   | RxBadPktLengthCnt : 0
   | RxMisorderedPktCnt : 800
   | RxLostPktCnt : 116800
   | RxBadPktChecksumCnt : 0
   | RxUnderrunSlipCnt : 0
   | RxOverrunSlipCnt : 0
   | RxLastVocoderType : 0
   | RxVocoderChangeCnt : 0
   | RxMaxDetectedPdv : 161 (in 125 us)
   | RxDecdrRate : 0
   | RxMaxJitterCurrentDelay : 162 (in 125 us)
   | RxJitterEstimatedDelay : 0 (in 125 us)
   | RxJitterEstimatedDelay : 0 (in 125 us)
   | RxJitterClkDriftingCorrectionCnt : 0
   | RxMaxJitterInitializationCnt : 1
   | RxCircularBufferWriteErrCnt : 0
   | RxApiEventCnt : 0
```
| TxCurrentVocoderType     : 0 |
| TxInPktCnt              : 125189952 |
| TxInBadPktPayloadCnt    : 0 |
| TxTimestampGapCnt       : 0 |
| TxTdmWriteErrCnt        : 0 |
| RxToneDetectedCnt       : 0 |
| RxToneRelayEventPktCnt  : 0 |
| RxToneRelayUnsupportedCnt : 0 |
| TxToneRelayEventPktCnt  : 0 |
| TxApiEventCnt           : 0 |
| TxNoRtpEntryPktDropCnt  : 0 |
| ConnectionWaitAckFlag   : 0 |
| RxMipsProtectionDropCnt : 0 |
| TxMipsProtectionDropCnt : 0 |
| CallTimerMsec           : 3130006 |

**NOTE:** The above mentioned are DSP 03 observed errors.
Octasic Tools Package

### E.1 Overview

Octasic provides tools that are used for diagnostic and debugging purposes. For this, users need to install the OCT-TOOLS package provided by SMART EC. OCT-TOOLS package is available separately for Windows and Linux OS. Users can choose and install based on the operating system they would use for debugging purpose.

The table below provides the available tools and a brief description about them.

<table>
<thead>
<tr>
<th>Directory Name</th>
<th>File Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>bin/tool</td>
<td>octconsole</td>
<td>A high-level command line interface (CLI) to Octasic products. octconsole provides a fast and simple way to interact with and test the target application.</td>
</tr>
<tr>
<td></td>
<td>octliveview</td>
<td>Application that displays a graphical view of the target Logical Objects.</td>
</tr>
<tr>
<td></td>
<td>octwireshark</td>
<td>Plug-ins for Wireshark (R) dissector to enable parsing of Octasic VocalloNet packets.</td>
</tr>
<tr>
<td></td>
<td>ethloopback_test</td>
<td>A companion application to the Octasic Hardware Debugging Tool (OCT1010hdt) for testing Ethernet loopback.</td>
</tr>
<tr>
<td>bin/tool/plugin</td>
<td></td>
<td>Contains the diagnostic tool application helpers and add-ins.</td>
</tr>
<tr>
<td>bin/tool/script</td>
<td></td>
<td>Contains the diagnostic tool runtime scripts and some sample scripts.</td>
</tr>
<tr>
<td>bin/oct1010</td>
<td>oct1010hdt</td>
<td>Contains the OCT1010 diagnostic tool platform-dependent applications.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A command line interface that provides debugging and testing options for various OCT1010 and OCT1010-ID interfaces</td>
</tr>
<tr>
<td>bin/install</td>
<td></td>
<td>Third-party application helpers used while configuring the package.</td>
</tr>
<tr>
<td>bin/wireshark</td>
<td>install.bat</td>
<td>Contains platform-dependent applications. Windows installer script for the Wireshark™ Octasic plug-ins.</td>
</tr>
<tr>
<td></td>
<td>install.sh</td>
<td>Linux environment script to install Octasic plug-ins for Wireshark™.</td>
</tr>
</tbody>
</table>
Octasic Tools Package
Appendix F

Install & Configure PCIE-8120 in MaxCore™

F.1 Overview

The section provides information on how to install the required SharpMedia™ PCIE-8120 RPMs and how to configure a PCIE-8120 card in a MaxCore™ MC3000 system.

MaxCore™ MC3000 is a platform for designing a highly scalable rack-mount appliance. The overall objective of this platform is to enable a wide range of solution providers to create their own competitive appliances and achieve the best time-to-market advantages. MaxCore differs from that of classical enterprise server in the sheer number of PCIe card slots available and its ability to implement many network connected servers within the same enclosure.

Refer to the data sheet for the MaxCore MC3000 platform for more information. Refer to Appendix G Related Documentation or consult your local SMART Embedded Computing sales representative for the availability of other variants.

For more information about MaxCore MC3000 platform, refer to the MaxCore Platform Data Sheet listed in Appendix G Related Documentation.

F.2 Installing Software and Configuring a PCIE-8120 Card in MaxCore

To install the software and configure a PCIE-8120 card inserted in a MaxCore system:

1. Untar the SSF_8120_<Release Version Number>.tgz file to the required location.

   $ tar zxvf SSF_8120_<Release Version Number>.tgz

After untarring the TGZ file, you will see the following files:

   mc3k_8120_software_update.sh
   pcie8120start
   ssf8120
   ssf8120.repo

2. Go to that location where the files were untarred and then run the following script.

   $ ./mc3k_8120_software_update.sh

   #################################################################
Installing Software and Configuring a PCIE-8120 Card in MaxCore

The complete installation procedure is divided into the following categories:

# 1. SSF-8120 Installation
# 2. SSF-8120 Uninstallation
# 3. Update
# "1" to install SSF-8120 and dependent rpms
# "2" to uninstall SSF-8120, which removes all SSF-8120, and dependent rpms.
# "3" to update SSF-8120, which updates SSF-8120 rpms.
# "4" to quit the installation

# Once the platform preparation is completed, it is suggested to the user not to uninstall the platform packages (dependent) until suggested. Only upgrade of SSF-MAXCORE packages is required when the user gets new release of SSF-MAXCORE package.

# Note: Please ensure that you have a known time zone on system to ensure proper processing of statistical data.

Installation Option:

1. SSF-8120 Installation
2. SSF-8120 Uninstallation
3. Update
4. Exit

Please enter your choice:

3. **Enter 1 for SSF-8120 Installation. The following actions are performed after completion of this task.**
   - Installs required RPMs along with Octasic and dependent RPMs
   - Configures DHCP and set up the environment to boot DSPs
   - Boots DSPs with Octasic Image
Installing Software and Configuring a PCIE-8120 Card in MaxCore

Sample Output

Loaded plugins: fastestmirror, langpacks
Cleaning repos: base extras ssf8120repo updates
Cleaning up everything
Loaded plugins: fastestmirror, langpacks
Cleaning repos: base extras ssf8120repo updates
Cleaning up everything
/tmp/8120
Loaded plugins: fastestmirror, langpacks
ssf8120repo
  | 2.9 kB  00:00:00
ssf8120repo/primary_db
  | 5.8 kB  00:00:00
Determining fastest mirrors
Resolving Dependencies
--> Running transaction check
 ---> Package octasic-sdk.x86_64 0:3.00.01-1A will be installed
 ---> Processing Dependency: sofia-sip for package: octasic-sdk-3.00.01-1A.x86_64
 ---> Processing Dependency: qt for package: octasic-sdk-3.00.01-1A.x86_64
 ---> Running transaction check
 ---> Package qt.x86_64 1:4.8.5-12.el7_2 will be installed
 ---> Processing Dependency: qt-settings for package: 1:qt-4.8.5-12.el7_2.x86_64
 ---> Package sofia-sip.x86_64 0:1.12.11-1 will be installed
 ---> Running transaction check
 ---> Package qt-settings.noarch 0:19-23.5.el7.centos will be installed
 ---> Finished Dependency Resolution
Dependencies Resolved
Installing Software and Configuring a PCIE-8120 Card in MaxCore

Transaction Summary

Install 1 Package (+3 Dependent packages)
Total download size: 50 M
Installed size: 100 M

Transaction Summary

Install 1 Package (+3 Dependent packages)
Total download size: 50 M
Installed size: 100 M

Total
188 MB/s | 50 MB 00:00:00
Running transaction check
Running transaction test
Transaction test succeeded
Running transaction
Installing: qt-settings-19-23.5.el7.centos.noarch
1/4
Installing: 1:qt-4.8.5-12.el7_2.x86_64
2/4
Installing: sofia-sip-1.12.11-1.x86_64
3/4
Installing Software and Configuring a PCIE-8120 Card in MaxCore

Installing: octasic-sdk-3.00.01-1A.x86_64
4/4
Verifying: sofia-sip-1.12.11-1.x86_64
1/4
Verifying: 1:qt-4.8.5-12.el7_2.x86_64
2/4
Verifying: qt-settings-19-23.5.el7.centos.noarch
3/4
Verifying: octasic-sdk-3.00.01-1A.x86_64
4/4
Installed:
octasic-sdk.x86_64 0:3.00.01-1A
Dependency Installed:
qt.x86_64:4.8.5-12.el7_2 qt-settings.noarch:0:19-23.5.el7.centos
sofia-sip.x86_64 0:1.12.11-1
Complete!
Loaded plugins: fastestmirror, langpacks
Loading mirror speeds from cached hostfile
Resolving Dependencies
---> Running transaction check
--- Package pcie8120.x86_64 0:1.6.3-MC_1 will be installed
---> Finished Dependency Resolution
Dependencies Resolved

Package Arch Version Repository Size

Installing:

pcie8120 x86_64 1.6.3-MC_1 ssf8120repo 207 k

Transaction Summary

Install 1 Package
Total download size: 207 k
Installing Software and Configuring a PCIE-8120 Card in MaxCore

Installed size: 1.3 M

Downloading packages:
Running transaction check
Running transaction test
Transaction test succeeded
Running transaction
Installing: pcie8120-1.6.3-MC_1.x86_64
1/1
Installing kernel module ... pcie8120.ko.el7.centos.x86_64.centos-7.2.1511
done.
Verifying: pcie8120-1.6.3-MC_1.x86_64
1/1
Installed:
    pcie8120.x86_64 0:1.6.3-MC_1
Complete!
PCIE-8120 Initialization
    fdev00.00 ... ok.
    fdev00.01 ... ok.
    fdev00.02 ... ok.
    updating caches ... done.
done.
pciutils-3.2.1-4.el7.x86_64
net-tools-2.0-0.17.20131004git.el7.x86_64
octasic-sdk-3.00.01-1A.x86_64
iptables-1.4.21-16.el7.x86_64
xinetd-2.3.15-12.el7.x86_64
tftp-server-5.2-12.el7.x86_64
ethtool-3.15-2.el7.x86_64
dhcp-4.2.5-42.el7.centos.x86_64
Generating configuration for boot VLAN ...
    processing card0: 26 enp26s0f0 enp26s0f1 enp26s0f2 ...
configuring network interface enp26s0f0.999 ... done.
setting up boot VLAN done.
Generating configuration for DHCP service ...
processing card0: 26 enp26s0f0 enp26s0f1 enp26s0f2 ...
generated pdev26-dhcpd.conf in /opt/bladeservices/etc
setting up DHCP service configuration done.
Setting up Firewall ...The service command supports only basic LSB
actions (start, stop, restart, try-restart, reload, force-reload,
status). For other actions, please try to use systemctl.
    done.
octSetup done.
Starting DSPs on card#0
  msw0: DSP0:  up
  msw0: DSP1:  up
  msw0: DSP2:  up
  msw0: DSP3:  up
  msw0: DSP4:  up
  msw0: DSP5:  up
  msw0: DSP6:  up
  msw0: DSP7:  up
  msw0: DSP8:  up
  msw0: DSP9:  up
  msw0: DSP10: up
  msw0: DSP11: up
Loaded plugins: fastestmirror, langpacks
Loading mirror speeds from cached hostfile
Resolving Dependencies
--> Running transaction check
---> Package ssf_maxcore_smcTLS_rel-8120.x86_64 0:1.1.0.13-el7
will be installed
--> Finished Dependency Resolution
Installing Software and Configuring a PCIE-8120 Card in MaxCore

Dependencies Resolved

Package Arch Version Repository Size

Installing:
ssf_maxcore_smcTLS_rel-8120 x86_64 1.1.0.13-el7 ssf8120repo 74 k

Transaction Summary

Install 1 Package

Total download size: 74 k
Installed size: 280 k
Downloading packages:
Running transaction check
Running transaction test
Transaction test succeeded
Running transaction
Installing: ssf_maxcore_smcTLS_rel-8120-1.1.0.13-el7.x86_64 1/1
Verifying: ssf_maxcore_smcTLS_rel-8120-1.1.0.13-el7.x86_64 1/1
Installed:
ssf_maxcore_smcTLS_rel-8120.x86_64 0:1.1.0.13-el7
G.1 SMART Embedded Computing Documentation

The documentation listed is referenced in this manual. Technical documentation can be found by using the Documentation Search at https://www.smartembedded.com/ec/support/ or you can obtain electronic copies of SMART EC documentation by contacting your local sales representative.

<table>
<thead>
<tr>
<th>Table G-1  SMART EC - Embedded Computing Publications</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Document Title</strong></td>
</tr>
<tr>
<td>SharpMedia™ PCIE-8120 Quick Start Guide</td>
</tr>
<tr>
<td>SharpMedia™ PCIE-8120 Data Sheet</td>
</tr>
<tr>
<td>MaxCore 3000 Platform Data Sheet</td>
</tr>
</tbody>
</table>

G.2 Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

<table>
<thead>
<tr>
<th>Table G-2  Related Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Organization</strong></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Octasic</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>